

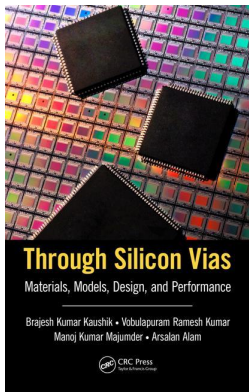
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Publisher: *CRC Press*

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Through Silicon Vias Materials, Models, Design, and Performance

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Publication details

<https://test.routledgehandbooks.com/doi/10.1201/9781315368825-4>

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Published online on: 26 Aug 2016

How to cite :- Brajesh Kumar Kaushik, Vobulapuram Ramesh Kumar, Manoj Kumar Majumder, Arsalan Alam. 26 Aug 2016, *Copper-Based Through Silicon Vias from: Through Silicon Vias, Materials, Models, Design, and Performance* CRC Press

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3

Copper-Based Through Silicon Vias

3.1 Introduction

The microelectronics industry has recently laid the foundation for the burgeoning advancement of information technology. Each electronic product launched is soon replaced by a more sophisticated successor that features enhanced functionality, connectivity, efficient power utilization, generally lower cost, and reduced size. Evolution of laptops is a good example that confirms this trend. Such enhancements have become so evident that the consumers expect the next-generation devices to be an upgrade over their previous versions in all aspects. To meet such anticipations, the electronics manufacturers are in continuous pursuit for higher integrations in order to incorporate more and more functionality within chips. Moreover, to reduce the power consumption and cost of the high-functionality chips, size reduction becomes essential.

The contribution of process technology scaling in semiconductors has played a major role in reducing the interconnection and transistor sizes over the past few decades. More than a billion transistors on a single chip have become a reality. However, such a high level of integration demands similar levels of design complexities. It is observed that the desired rate of scaling is not being achieved for transistor channel lengths of less than 20 nm [1]. This is because the process technology scaling is facing challenges such as increased leakage current and power consumption, process variability, lithography limitations, and reduced production yield. In spite of the immense efforts being made to overcome these issues, it has become evident that scaling alone cannot keep up with the required trend of integration. Development in chip packaging technologies has provided assistance toward increased integration. The development of chip packaging from its early days to the present enhancements has been discussed in Chapter 1. The advantages provided by both process technology scaling and chip packaging techniques have almost reached their maximum potential. However, increasing the demand for maintaining the trend of developments in electronic products is swiftly becoming a necessity in our lives. Therefore, it has become evident that an alternate technology to develop microelectronic systems is utmost required.

The development of three-dimensional integrated circuits (3D ICs) with through silicon vias (TSVs) has provided a promising platform to satisfy the

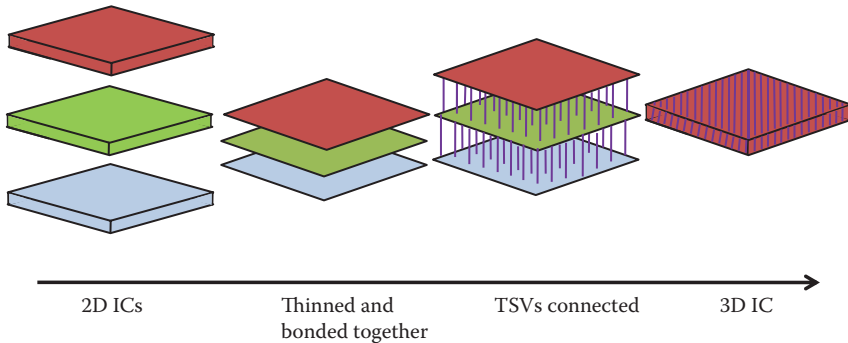


FIGURE 3.1

A detailed step-by-step view showing that a 3D IC is made from 2D ICs that are reduced in thickness, bonded together, and finally connected via Cu-based TSVs.

development in accordance with Moore's law. The Cu filler material used in TSVs plays an important role in providing the desired quality of TSVs. Cu provides lower stress, void-free filling, and good thermal cycling performance, conductivity, and electrical current-carrying capability [2]. Some of the other TSV filler materials used are conductive polymer pastes, gold (Au), polysilicon, and tungsten (W) [3–5]. However, there are issues of testing, packaging, and fabrication of these filler materials. The development of a 3D IC with Cu-based TSVs from two-dimensional integrated circuits (2D ICs) is shown in Figure 3.1. TSVs provide electrical connections between oxide or through silicon tiers in vertical directions. They decrease the distance between connections and thus provide reduced signal delay and power consumption, higher bandwidth, and compact and reliable connection paths along with easing design complexities. It is important to discuss the various aspects of Cu-based TSVs because Cu is the most common filler material because of its economic feasibility and excellent electrical properties.

The rest of the chapter is divided into four sections. Section 3.2 provides the details of the physical configuration of Cu-based TSVs. Section 3.3 discusses the various equivalent electrical models of Cu-based TSVs such as TSVs with bumps, metal semiconductor (MES) ground structure, and ohmic contact in silicon interposer. Section 3.4 analyzes the performance of Cu-based TSVs in terms of propagation delay, power dissipation, crosstalk-induced delay, frequency response, and bandwidth. Finally, Section 3.5 provides a summary of this chapter.

3.2 Physical Configuration

The 3D stacking technology plays a significant role in deciding the geometry of the TSV. The different TSV physical structures such as circular, tapered, annular, square, and rectangular are shown in Figure 3.2. To evaluate the

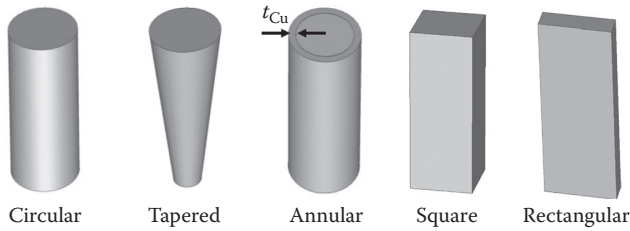


FIGURE 3.2
Different physical structures of TSVs.

shape impacts on the performance of TSVs, we must keep the cross-sectional areas constant on the top plane. Xu et al. [5] analyzed the performance evaluation between the different TSV shapes by comparing the loss parameters. The return loss and insertion loss are shown in Figure 3.3a and b, respectively. It can be observed among all the shapes of TSVs, the tapered shape TSV has the smallest return loss and insertion loss. This is due to the fact that the tapered shape TSV has a relatively low capacitance value because of its reduced surface area. To reduce the fabrication cost, the annular structured TSVs are preferable due to less amount of filler material needed for their fabrication.

The TSVs can be used for power supply/ground, clock, or analog and digital signals [1]. In general, the geometry of all TSVs within a chip is the same to provide ease in optimizing the 3D technology process. After choosing a TSV technology, the only flexibility in the electrical characteristics of TSV design is the use of more TSVs in parallel to each other within the same link. This can be helpful in power supply networks that require low-resistance interconnects and high DC current capability. Connecting the TSVs in parallel results in the decrease of resistance in power/ground links of the stacked dies. It also results in the increase of the TSV parasitic capacitance. The TSV structure, in terms of both materials and geometry, significantly contribute to the parasitic values of the TSV.

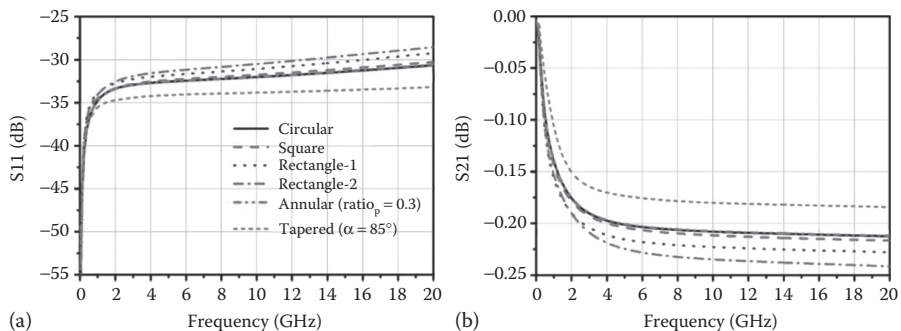


FIGURE 3.3
Impact of TSV shapes on electrical performance (a) S11 and (b) S21. (From Xu, Z. and Lu, J.-Q., *IEEE Transactions on Components, Packaging and Manufacturing*, 1, 154–162, 2011. With Permission.)

The placement of TSVs within 3D ICs is a complex process of additional process steps and may affect the reliability of the chip. The typical range of TSV height is several hundreds of micrometers and that of TSV diameter is several tens of micrometers. Discussing the physical configuration of TSVs along with involving physical characterization will bring out a clear understanding of TSV structures. The fabrication of TSVs first involves the creation of holes into the Si by etching. The liner oxide (SiO_2) is then deposited into the hole followed by the diffusion barrier layers (TaN/Ta or TiN/Ti). The important Cu seed layers are then deposited. To properly fill the TSVs with Cu, electrochemical deposition is used. For Cu recrystallization, thermal annealing is performed. This step is required to provide resistance against electromigration and stress-generated degradation, and to improve the conductance of the TSVs. To isolate the TSVs and remove the excess Cu, chemical–mechanical polishing is performed. After processing, it is required that the surface of the wafer in the region around the TSVs should be flat in order to properly integrate the TSVs within the chips. Moreover, it is essential to assess the reliability of the diffusion barriers within TSVs. This is because the metal contamination in transistors, particularly in the active regions, can result in failure or severe performance degradations of electrical devices.

The uniformity in cross section of TSVs is an important criterion for providing overall reliability. As the TSVs are quite large in size, their preparation can be very time consuming, requiring several hours for every cross section. The etch profile can be evaluated by a cleave through the TSV [6]. A good-quality cross-sectional preparation is difficult if the metal fill in TSVs is completed. This is because the metal layers will be ripped out or deformed during cleaving. The cross section is required for such samples for the purpose of measuring the diffusion barrier layer thickness. The cross sections in such cases can be prepared via the techniques of broad-beam argon ion milling, focused ion beam milling, or mechanical polishing [6].

3.3 Modeling of Cu-Based TSVs

3D field solvers require high computational time; therefore, it is essential to develop an electrical equivalent model of TSV to reduce the computational time and for a better physical insight. Moreover, the equivalent models have to be analytical, upgradable, reducible, and must consider the physical dimensions and material properties; hence, if the material properties or the dimensions are scaled, the model gets adapted to the changed parasitic values accordingly. This allows for easier implementation and modifications in the TSV design structures.

3.3.1 Scalable Electrical Equivalent Model of Coupled TSVs with Bumps

A scalable electrical equivalent model of coupled TSVs is presented in this section. As the model is obtained through the physical structure, each parasitic component is clearly expressed through its physical meaning with the help of the closed-form equations. To obtain the scalable model, the analytical equations are derived based on the material properties and structural parameters.

Kim et al. [7] proposed a high-frequency scaled electrical model for the analysis of coupled TSVs. The proposed model considers not only the TSVs but also the bumps that are the additional components for 3D-based TSV design. The structure of signal and ground TSVs with bumps are shown in Figure 3.4, in which the bumps provide connection between the stacked heterogeneous dies. Depending on the configuration, the electrical equivalent model of a pair of Cu TSVs is shown in Figure 3.5 [7].

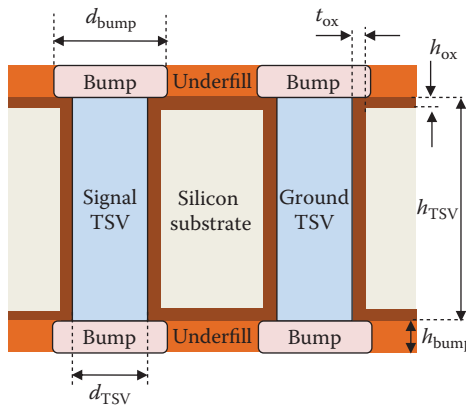


FIGURE 3.4 Structure of signal TSV and ground TSV with bumps.

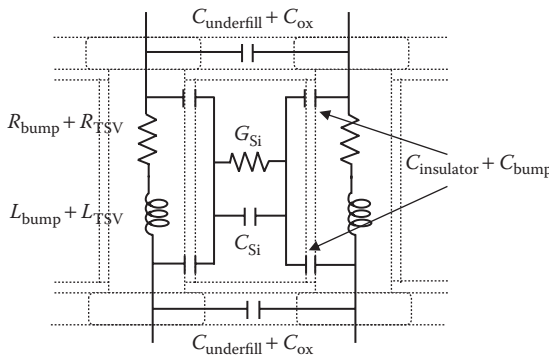


FIGURE 3.5 Electrical equivalent model of signal and ground TSVs.

The resistances of the TSV and bump are represented by R_{TSV} and R_{bump} respectively. At high frequencies, the current flows primarily on the surface of the conductor with an exponential reduction in current density toward the depth of the conductor. Therefore, the overall resistance of the conductor is substantially reduced at high frequencies. The depth of penetration in which the current falls off to e^{-1} of its value near the surface is known as skin depth (δ). This skin depth is accounted for in the modeling of R_{TSV} and R_{bump} at high frequencies. The resistances are determined by the resistivity of the TSV and bump, ρ_{TSV} and ρ_{bump} ; the radius of the TSV and bump, r_{TSV} and r_{bump} ; and the height of the TSV and bump, h_{TSV} and h_{bump} , respectively. The skin depth determines the material properties such as permittivity, resistivity of the TSV filler material, and the operating frequencies. The proximity factor, k_p , is determined by the ratio of distance between the two TSVs (p_{TSV}) and their radii (r_{TSV}) [8]. The resistance of the TSV can be expressed as

$$R_{\text{TSV}} = \sqrt{(R_{\text{dc,TSV}})^2 + (R_{\text{ac,TSV}})^2} \quad (3.1)$$

where:

$$R_{\text{dc,TSV}} = \rho_{\text{TSV}} \times \frac{h_{\text{TSV}}}{\pi \times r_{\text{TSV}}^2}$$

$$R_{\text{ac,TSV}} = k_p \left(\rho_{\text{TSV}} \times \frac{h_{\text{TSV}}}{2\pi \times r_{\text{TSV}} \times \delta_{\text{TSV}} - \pi \delta_{\text{TSV}}^2} \right) \quad (3.2)$$

$$\delta_{\text{TSV}} = \sqrt{\frac{\rho_{\text{TSV}}}{\pi \times f \times \mu_{\text{TSV}}}} \quad (3.3)$$

The resistance of the bump is expressed as

$$R_{\text{bump}} = \sqrt{(R_{\text{dc,bump}})^2 + (R_{\text{ac,bump}})^2} \quad (3.4)$$

where:

$$R_{\text{dc,bump}} = \rho_{\text{bump}} \times \frac{h_{\text{bump}}}{\pi \times r_{\text{bump}}^2}$$

$$R_{\text{ac,bump}} = k_p \left(\rho_{\text{bump}} \times \frac{h_{\text{bump}}}{2\pi \times r_{\text{bump}} \times \delta_{\text{bump}} - \pi \delta_{\text{bump}}^2} \right) \quad (3.5)$$

$$\delta_{\text{bump}} = \sqrt{\frac{\rho_{\text{bump}}}{\pi \times f \times \mu_{\text{bump}}}} \quad (3.6)$$

The parasitic inductance has started to play an important role in the analysis of TSV performance due to the adoption of low-resistance TSV materials and high operating switching frequencies. The TSV inductance (L_{TSV}) and bump inductance (L_{bump}) are expressed as [9]

$$L_{\text{TSV}} = \frac{1}{2} \left[\frac{\mu_0 \mu_r, \text{TSV}}{2\pi} \times h_{\text{TSV}} \times \ln \left(\frac{p_{\text{TSV}}}{r_{\text{TSV}}} \right) \right] \quad (3.7)$$

$$L_{\text{bump}} = \frac{1}{2} \left\{ \frac{\mu_0 \mu_r, \text{bump}}{2\pi} \times h_{\text{bump}} \times \ln \left(\frac{p_{\text{bump}}}{r_{\text{bump}}} \right) \right\} \quad (3.8)$$

To avoid the signal flow from the TSV conductor to the silicon substrate, an insulating layer surrounding the TSV metal layer is necessary. Thus, an insulating capacitance is formed between the metal TSV and the semiconductor substrate. The $C_{\text{insulator}}$ is determined by the h_{TSV} , the height of the insulating layer h_{ox} , r_{TSV} , and the permittivity of the insulating layer. Using the coaxial cable capacitance model, the $C_{\text{insulator}}$ is derived as

$$C_{\text{insulator}} = \frac{1}{2} \left[2\pi \times \epsilon_0 \epsilon_r, \text{insulator} \times \frac{h_{\text{TSV}} - 2h_{\text{ox}}}{\ln \left(\frac{r_{\text{TSV}} + t_{\text{ox}}}{r_{\text{TSV}}} \right)} \right] \quad (3.9)$$

Due to the overlapping region of bump-to-silicon substrate of the upper side as well as the lower side, a capacitance is formed named as C_{bump} , and it must be added to the $C_{\text{insulator}}$ as shown in Figure 3.5. The C_{bump} is modeled as a parallel plate capacitor and can be expressed as

$$C_{\text{bump}} = \epsilon_0 \epsilon_r, \text{insulator} \times \frac{\pi \times \left[r_{\text{bump}}^2 - (r_{\text{TSV}} + t_{\text{ox}})^2 \right]}{h_{\text{ox}}} \quad (3.10)$$

The capacitance between the signal TSV and the ground TSV forms the insulating layer, C_{ox} , and the capacitance between the signal bump and the ground bump forms the underfill, $C_{\text{underfill}}$. These capacitances are modeled as parallel-wire capacitances and can be expressed as [7]

$$C_{\text{ox}} = \frac{\pi \times \epsilon_0 \epsilon_r, \text{insulator}}{\cosh^{-1} \left(\frac{p_{\text{TSV}}}{2r_{\text{TSV}}} \right)} \times h_{\text{ox}} \quad (3.11)$$

$$C_{\text{underfill}} = \frac{\pi \times \epsilon_0 \epsilon_r, \text{underfill}}{\cosh^{-1} \left(\frac{p_{\text{TSV}}}{2r_{\text{bump}}} \right)} \times h_{\text{bump}} \quad (3.12)$$

Due to the semiconductor silicon substrate, there are conductance and capacitance between the signal and ground TSVs. Using the parallel-wire capacitance model, the C_{si} is represented as

$$C_{si} = \frac{\pi \times \epsilon_0 \epsilon_{r,si}}{\cosh^{-1}\left(\frac{p_{TSV}}{2r_{TSV}}\right)} \times (h_{TSV} - 2h_{ox}) \quad (3.13)$$

Using the relationship between the capacitance and the conductance, $C_{si}/G_{si} = \epsilon_{si}/\sigma_{si}$ [10], the conductance can be expressed as

$$G_{si} = \frac{\pi \times \sigma_{si}}{\cosh^{-1}\left(\frac{p_{TSV}}{2r_{TSV}}\right)} \times (h_{TSV} - 2h_{ox}) \quad (3.14)$$

Because all the parasitic elements are expressed in terms of physical dimensions and material properties, the model can be used to estimate the TSV behavior with different material properties and dimensions.

3.3.2 Modeling of Multicoupled TSVs

In a realistic scenario, we come across multiple numbers of TSVs; consider a TSV that is present in the vicinity of the reference TSV pair as shown in Figure 3.6. The conventional formulas derived in Section 3.3.1 cannot be applied for this configuration because the substrate capacitance varies in presence of other TSVs. Therefore, this section is focused on the modeling of substrate capacitance and conductance of multicoupled TSVs. C. R. Paul [11] considered the similar problem and calculated the capacitance matrix for ribbon cables. Using the same approach, the capacitance and conductance matrix can be calculated as

$$[C] = \mu_0 \epsilon_{si} [L]^{-1} \quad (3.15)$$

$$[G] = \mu_0 \sigma_{si} [L]^{-1} \quad (3.16)$$

where L is the inductance matrix and each element is expressed as

$$L_{ii} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0}^2}{r_i r_0}\right) \quad (3.17)$$

$$L_{ij} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0} d_{j0}}{d_{ij} r_0}\right) \quad (3.18)$$

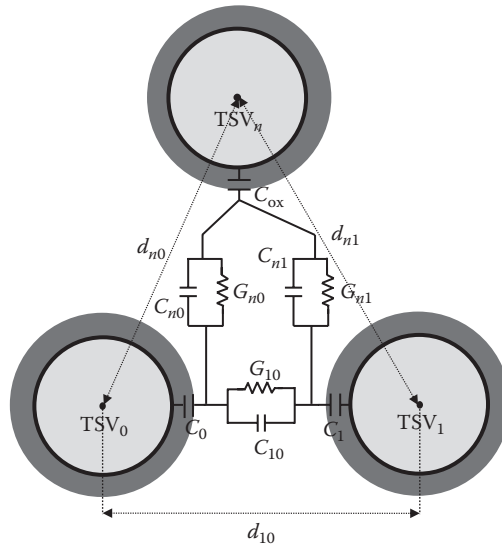


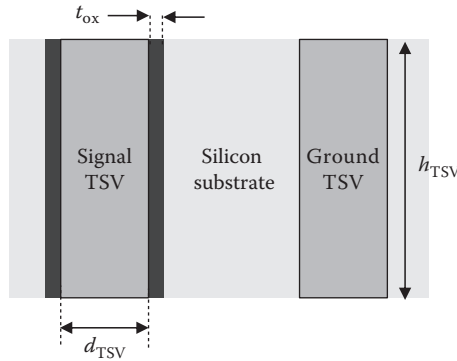
FIGURE 3.6
Conductance and capacitance modeling of coupled multiple TSVs.

3.3.3 Modeling of Coupled TSVs with MES Ground Structure

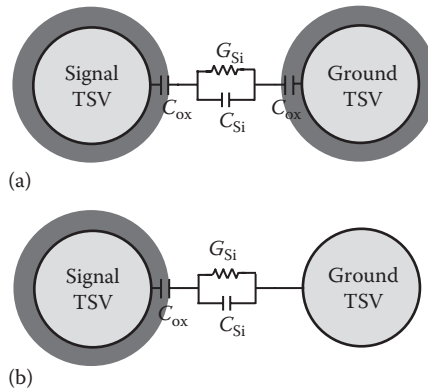
The conventional TSV structure discussed in Section 3.3.1 is the metal–insulator–semiconductor (MIS) configuration. Process development on TSVs are now gearing up toward the new type of configuration named as MES type as shown in Figure 3.7, and the top view of the MES structure is shown in Figure 3.8. In the MES configuration, the insulating layer around the ground TSV is removed as shown in Figure 3.7. The MES ground TSV behaves as a ground plug to reduce the noise in the substrate [12]. Additionally, these MES TSVs behave like a thermal via that can effectively transfer heat. However, the MES TSVs are not preferred for signal and power TSVs, because they deteriorate due to the formation of an ohmic contact to the silicon substrate. Engin et al. [13] observed that the MES TSVs completely eliminate the capacitive crosstalk in a low-frequency mode. However, the reduction in crosstalk is less significant for shorter TSV heights, because the line resistance of the ground TSV dominates over coupling parasitics.

3.3.4 Modeling of TSVs with Ohmic Contact in Silicon Interposer

Engin et al. [13] assumed a perfect ohmic contact between the metal and the silicon substrate as discussed in Section 3.3.3. In general, the silicon substrate of an IC is usually grounded, and therefore, the contact resistance and capacitance at the interface of metal–silicon can be safely ignored. However, because the silicon interposer is not often grounded, the resistances (R_{contact} and R_{region}) and capacitance (C_{doping}) need to be

**FIGURE 3.7**

Cross-sectional view of MIS signal TSV and MES ground TSV.

**FIGURE 3.8**

Top view of (a) conventional MIS structure and (b) modified structure with MIS signal TSV and MES ground TSV.

included during the modeling of TSVs in silicon interposer. This section describes the effect of contact resistance, doping resistance, and capacitance on the performance of MES TSVs [14]. A signal–ground–signal (SGS) TSV is shown in Figure 3.9. The ground TSV is used as a shield between the two signal TSVs by creating a Faraday cage [15]. However, the ground TSV with doping region around it provides a better signal reference to the signal TSVs due to significantly reduced contact resistance. Therefore, during the fabrication of TSVs, a doping region is created around the ground TSV to reduce its contact resistance. Thus, the doping resistance (R_{region}) and capacitance (C_{doping}) must be incorporated into the electric equivalent model as shown in Figure 3.10.

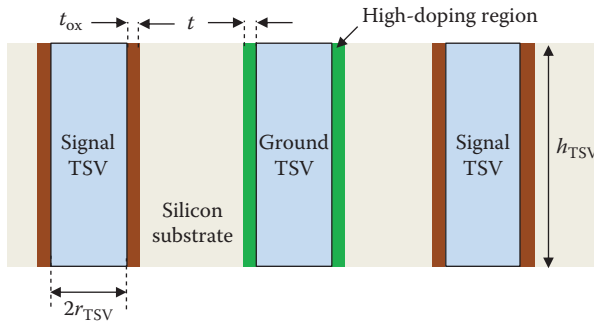


FIGURE 3.9 Signal-ground-signal TSV structure with doping region around the ground TSV.

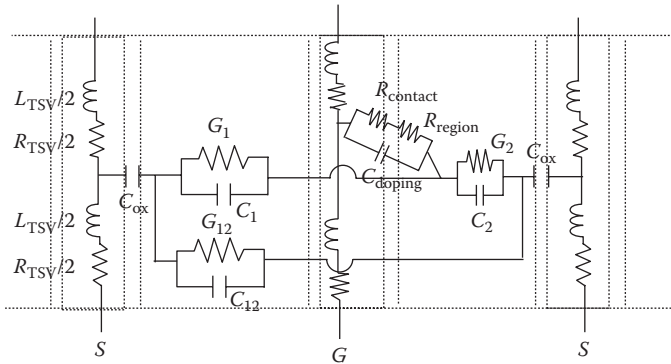


FIGURE 3.10 Electrical equivalent model of signal-ground-signal TSV with ohmic contact around the ground TSV.

The contact resistance must be added to the R_{region} due to the work function difference between the metal and the semiconductor and can be modeled as

$$R_{\text{contact}} = \frac{\rho_c(N_a)}{2\pi r_{\text{TSV}} h_{\text{TSV}}} \quad (3.19)$$

where:

h_{TSV} is the height of the TSV

$\rho_c(N_a)$ is the contact resistivity that is obtained from the doping concentration

The resistance and capacitance of the doping region can be expressed as

$$R_{\text{region}} = \frac{\rho}{2\pi h_{\text{TSV}}} \ln\left(\frac{r_{\text{TSV}} + t}{r_{\text{TSV}}}\right) \quad (3.20)$$

$$C_{\text{doping}} = \frac{\epsilon_{\text{Si}} h_{\text{TSV}}}{\ln\left(\frac{r_{\text{TSV}} + t}{r_{\text{TSV}}}\right)} \quad (3.21)$$

The performance of SGS TSVs with and without doping regions was analyzed in [15]. It is observed that the doping region around the ground TSV significantly reduces the near-end coupling noise. This reduction is primarily dependent on the concentration profile of the doping region.

3.4 Performance Analysis of Cu-Based TSVs

This section analyzes the performance of Cu-based TSVs for different via heights. The performance of Cu-based TSVs is compared in terms of propagation delay, power dissipation, crosstalk-induced delay, frequency, and bandwidth analysis. Circuit simulations are performed based on the electrical equivalent model to investigate the performance analysis of TSVs.

3.4.1 Propagation Delay and Power Dissipation

The schematic view of Cu-based TSV that is driven by a complementary metal oxide semiconductor (CMOS) driver and terminated by a capacitive load is shown in Figure 3.11. The material properties considered are shown in Table 3.1. The equivalent load capacitance is considered as 45 aF. The propagation delay and power dissipation for varying heights of Cu-based TSV are shown in Figure 3.12.

It can be observed from Figure 3.12 that as the TSV height increases, the delay and power dissipation also increase. There is almost a linear dependence of delay and power dissipation with the TSV height. This is because the TSV parasitics increase with the TSV height, and both the delay and the power dissipation linearly depend on the TSV parasitics.

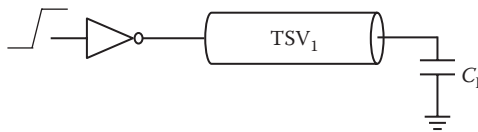


FIGURE 3.11

Schematic view of Cu-based TSV driven by a CMOS driver and terminated by capacitive load.

TABLE 3.1

Material Properties of Cu-Based TSVs

Symbol	Value	Symbol	Value
σ_{Si}	10 S/m	$\mu_{r,\text{RDL}}$	1
$\epsilon_{r,\text{ox}}$	4	$\mu_{r,\text{Bump}}$	1
$\epsilon_{r,\text{Si}}$	11.9	$\mu_{r,\text{TSV}}$	1
ρ_{RDL}	$1.68 \times 10^{-8} \Omega\text{m}$	$\epsilon_{r,\text{Underfill}}$	7
ρ_{Bump}	$1.68 \times 10^{-8} \Omega\text{m}$	$\epsilon_{r,\text{ox,bot}}$	4
ρ_{TSV}	$1.68 \times 10^{-8} \Omega\text{m}$	$\epsilon_{r,\text{IMD}}$	4

Source: Kim, J. et al., *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(2), 181–195, 2011.

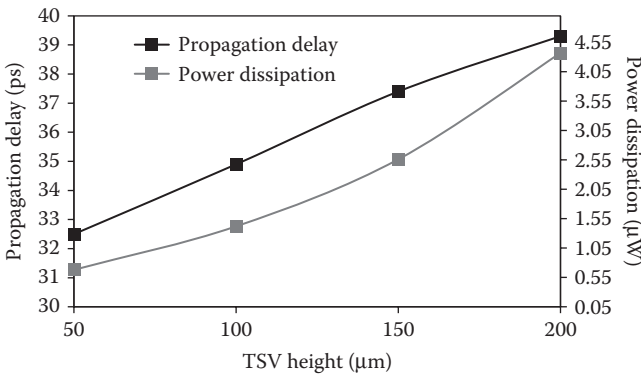


FIGURE 3.12

Propagation delay and power dissipation of Cu-based TSVs for varying heights.

3.4.2 Crosstalk-Induced Delay

The capacitive coupling is generated between the two TSVs, if they are placed in close proximity to each other [16]. Figure 3.13 shows two Cu-based TSVs in close proximity to each other. As a result, the capacitive coupling is generated as shown in Figure 3.14. The crosstalk noise is analyzed in the following two cases: (1) in-phase delay, in which the coupled TSVs are simultaneously switched in the same phase and (2) out-phase delay, in which the coupled TSVs are simultaneously switched in the opposite phase.

The crosstalk-induced propagation delay is analyzed at different TSV heights and shown in Figure 3.15. The mutual capacitance is considered in the line capacitance during out-phase switching of coupled TSVs, and it is neglected during the in-phase switching of coupled TSVs. This is due to the effect of Miller coupling capacitance. The Miller capacitance largely

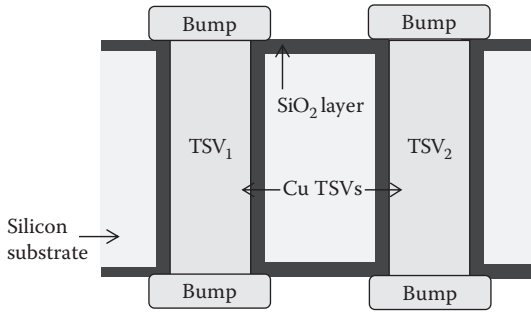


FIGURE 3.13
Physical configuration of a pair of Cu-based TSVs.

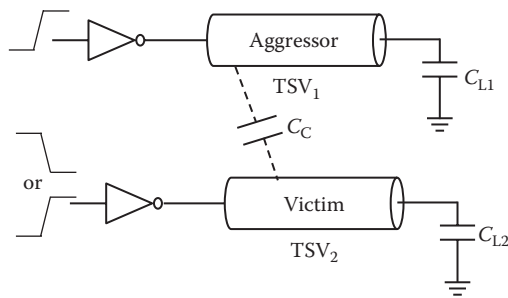


FIGURE 3.14
Schematic view of capacitively coupled TSV lines.

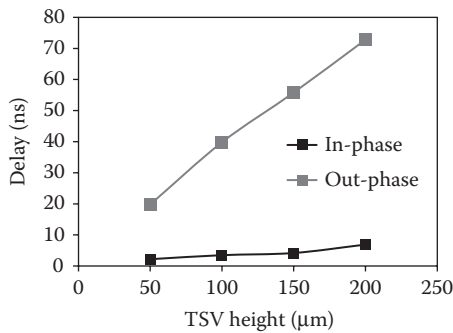


FIGURE 3.15
Comparison of crosstalk-induced dynamic in-phase and out-phase propagation delay between coupled TSVs.

influences the signal propagation when the coupled lines transit in the opposite direction, whereas it has no effect when the coupled lines transit in the same direction [17]. Therefore, it can be observed that the out-phase delay is higher than the in-phase delay.

The nonlinear dependence of propagation delay on the TSV height can be observed from Figure 3.15. The delay time of the driver-TSV-load (DTL) system is dependent on the parasitics of the driver, the TSV line, and the load. The TSV parasitics are linearly dependent on the height of the TSV, whereas the driver and load parasitics are not dependent on the TSV height. Also, the driver response to different TSV lines and load parasitics is nonlinear. Therefore, the cumulative effect of the TSV height on the delay time is nonlinear [17].

3.4.3 Frequency Response and Bandwidth Analysis

This section analyzes the frequency response and bandwidth of Cu-based TSVs with the help of transfer function (TF) of the DTL system, as shown in Figure 3.16. The TF accurately considers the driver resistance, the driver capacitance, and the via parasitic, as shown in Table 3.2.

To obtain the overall gain (V_{out}/V_{in}), the DTL of Figure 3.16 is represented as a cascaded connection of several two-port networks, as shown in Figure 3.17. The best choice of the two port parameters is the $ABCD$ parameter. The $ABCD$ matrix parameters of each two-port network are represented as g_1, g_2 ,

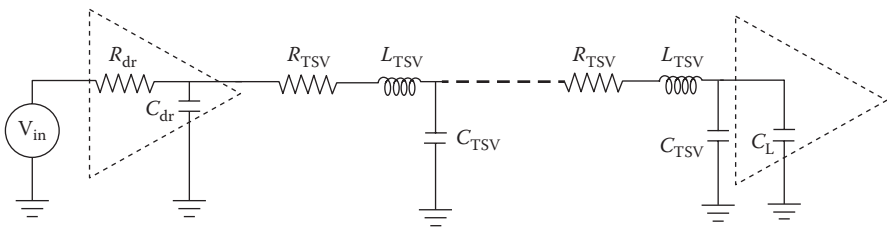


FIGURE 3.16

A DTL system. R_{dr} and C_{dr} represent the driver resistance and capacitance, respectively.

TABLE 3.2

Equivalent Parasitics of Cu-Bundled TSVs

Via Parasitics	Values
R_{TSV} (m $\Omega/\mu\text{m}$)	7.1
L_{TSV} (pH/ μm)	1.05
C_{TSV} (fF/ μm)	0.45
R_{dr} (Ω)	292.36
C_{dr} (aF)	45.51

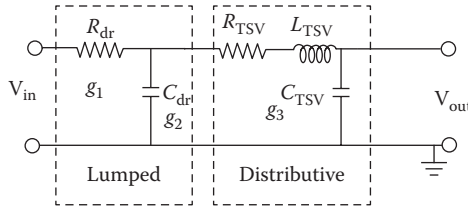


FIGURE 3.17
Cascaded connection of Figure 3.16.

and g_3 . Telegrapher’s equation of a distributed transmission line is used to obtain the $ABCD$ matrix parameter (gain) g_2 .

Using the transmission matrix parameter for a uniform RLC transmission TSV of height h , the resultant matrix parameter of the DTL configuration can be expressed as [18,19]

$$\begin{aligned}
 T_{\text{result}} &= g_1 \cdot g_2 \cdot g_3 \\
 &= \begin{bmatrix} 1 & R_{\text{dr}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_{\text{dr}} & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma nx) & Z_0 \sinh(\gamma nx) \\ 1/Z_0 \sinh(\gamma nx) & \cosh(\gamma nx) \end{bmatrix} \\
 &= \begin{bmatrix} A & B \\ C & D \end{bmatrix}
 \end{aligned} \tag{3.22}$$

In the above equation, Z_0 , γ , n , and x are the characteristic impedance, propagation constant, number of distributed segments, and length of each segment, respectively.

Now, using Equation 3.22, the distributed TF of the DTL can be expressed as [17]

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \text{TF} = \frac{1}{A + sC_L B} \tag{3.23}$$

where:

$C_L = 10$ fF is the load capacitance

A and B are the coefficients

The derivation of the coefficients A and B can be derived from Equation 3.22.

The TF of Equation 3.23 is used to obtain the cutoff frequency (f_c) that primarily depends on the via parasitics. The parasitic values are obtained for a fixed via radius of $2.5 \mu\text{m}$. The second-order TF of the DTL system can be expressed as

$$TF = \frac{1}{a_0 + a_1s + a_2s^2} \quad (3.24)$$

where the coefficients a_0 , a_1 , and a_2 can be derived from Equation 3.23.

Substituting $a_0 = 1$, the roots of Equation 3.24 can be expressed as

$$s_1 = \frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2a_2} \quad (3.25)$$

and

$$s_2 = \frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2a_2} \quad (3.26)$$

Therefore, the cutoff frequency, f_c , can be obtained as

$$f_c = \frac{1}{2\pi} \sqrt{\frac{(2a_2 - a_1^2) + \sqrt{(2a_2 - a_1^2)^2 + 4a_2^2}}{2a_2^2}} \quad (3.27)$$

For a fixed TSV radius of 2.5 μm , Figure 3.18 shows the plots for the frequency response of DTL at TSV heights of 30, 60, 90, and 120 μm , respectively. It is

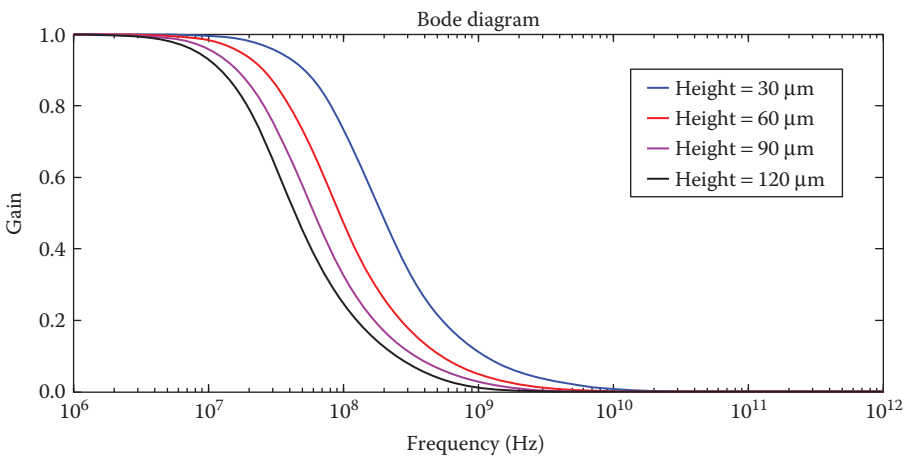


FIGURE 3.18

Frequency response of Cu-based TSVs for different TSV heights.

TABLE 3.3

Cutoff Frequency of Cu-Based TSVs for Different Heights

TSV Height (μm)	Cutoff Frequency (GHz) for Cu-Based TSVs
30	0.856
60	0.158
90	0.036.8
120	0.00912

observed that the longer TSVs exhibit smaller bandwidth. It is due to comparatively higher values of R and C with the increase in the TSV height. It leads to form an RC low-pass filter that has a bandwidth close to the cutoff frequency, $f_c = 1/2\pi RC$. Table 3.3 presents the cutoff frequency of Cu-based TSVs for different TSV heights.

3.5 Summary

TSV-based 3D IC technology has become inevitable to maintain the trend of chip development in accordance with Moore's law. The TSVs provide shorter interconnections between the chip and the substrate, thus improving the electrical performance of the system through decrease in power dissipation and propagation delay. An insight into the physical configuration along with physical characterization of Cu-based TSVs has been provided in this chapter. The typical range of the TSV height is several hundreds of micrometers and the TSV diameter is several tens of micrometers. For performance analysis, electrical modeling of Cu-based TSVs is discussed. The scalable electrical equivalent model of coupled TSVs is presented, which can be represented by the lumped model-based analytical equations. The modeling of TSVs with bumps, coupled TSVs with MES ground structure, TSVs with ohmic contact in silicon interposer is also provided. Based on the electrical modeling of TSVs with bumps, the performance analysis of the Cu-based TSVs is carried out. The performance analysis comprised the propagation delay, power dissipation, comprehensive crosstalk analysis in terms of functional, dynamic in-phase and out-phase crosstalk, and finally the frequency and bandwidth analyses. It was observed that the delay and power dissipation increase, whereas the bandwidth decreases with the TSV height.

Multiple Choice Questions

- Which of the following material is used as a TSV filler material?
 - Polymer paste
 - Silicon dioxide
 - Polysilicon
 - All of the above
- In which direction TSVs provide electrical connection between oxide and tiers?
 - Horizontal direction
 - Vertical direction
 - No connection
 - All directions
- Which of the following TSV shapes has smallest insertion loss and return loss?
 - Circular
 - Tapered
 - Annular
 - Square
- Which of the following TSV shape has the lowest fabrication cost?
 - Rectangular
 - Tapered
 - Annular
 - Circular
- Arrange the following in the correct order of fabrication steps used in TSV fabrication:
 - Etching =>SiO₂ deposition =>diffusion =>Cu seed layer deposition
 - Cu seed layer deposition =>SiO₂ deposition =>diffusion =>etching
 - Etching =>Cu seed layer deposition =>diffusion =>SiO₂ deposition
 - Diffusion =>SiO₂ deposition =>etching =>Cu seed layer deposition
- The process step used in preparing the cross section of TSV is
 - Broad-beam argon ion milling
 - Focused ion beam milling
 - Mechanical polishing
 - None of the above

7. The doping region is created around the ground TSV
 - a. To reduce ground resistance
 - b. To increase ground resistance
 - c. To provide better signal reference
 - d. Both b and c
 8. If the height of the TSV is increased, the contact resistance would
 - a. Increase
 - b. Decrease
 - c. Remain constant
 - d. None of the above
 9. If the height of the TSV is increased, the bandwidth would
 - a. Increase
 - b. Decrease
 - c. Remain constant
 - d. None of the above
 10. The MES ground TSV behaves as a ground plug to reduce
 - a. Noise
 - b. Resistivity
 - c. Conductivity
 - d. Capacitance
-

Short Questions

1. Why the desired rate of scaling is not being achieved for transistor channel lengths of less than 20 nm?
2. Why Cu is used as a filler material in TSVs than W?
3. Why the tapered shape TSV has the smallest return loss and insertion loss?
4. What are the process steps used for filling the Cu and to recrystalline it?
5. Why the good-quality cross-sectional preparation is difficult if the metal fill in TSVs is completed?
6. Draw the power delay product curve with respect to the TSV diameter.
7. Explain how the crosstalk noise is affected with respect to pitch distance.

8. Write the expression of the cutoff frequency for DTL and explain how the bandwidth is changing with the height of TSV?
 9. What is skin depth and how the resistance is affected by it?
 10. What is proximity factor?
-

Long Questions

1. Explain the physical configuration of TSV and explain its impact on electrical performance?
 2. Explain the electrical model of coupled TSV and also describe its resistance and insulated capacitance?
 3. Derive the expression for substrate conductance in coupled TSVs?
 4. Explain multicoupled TSV with its conductance and capacitance modeling?
 5. Explain the frequency response for Cu-based TSV and derive the expression for its bandwidth.
-

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