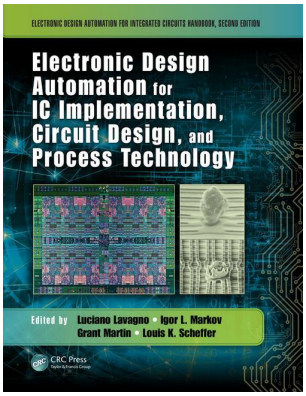

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology

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Exploring Challenges of Libraries for Electronic Design

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Exploring Challenges of Libraries for Electronic Design

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12.1 INTRODUCTION

Explaining how to best design libraries is usually a difficult task. We all know that a library is a collection of design behavior models at specific points in the design process, but in order to fully understand what it means to design libraries, we have to explore the intricacies and challenges of designing libraries. This includes examining what it means to design libraries, understanding the background, exploring the design process, and, perhaps, even analyzing the business models for libraries.

12.2 WHAT DOES IT MEAN TO DESIGN LIBRARIES?

Good designers must optimize constraints to achieve market requirements in terms of a finite number of cost functions. For example, they have to consider costs, performance, features, power consumption, quality, and reliability. These considerations are pretty universal for any design—even if you were designing a car, cell phone, or toaster.

On top of the traditional design constraints, the dramatic shortening of product life cycles also impacts design engineers. Often, this concern results from the dominance of consumer applications in the marketplace. The components of this trend are as follows:

- Hardware continues to be commoditized.
- Spiraling design costs lead to an increasing use of design platforms.
- Original device manufacturers (ODMs) build private label hardware (e.g., Wal-Mart).
- Original equipment manufacturers (OEMs) differentiate software and build brand value (e.g., Dell).
- Value is created through algorithms, system architecture, and software.
- Partitioning hardware and software has become the key decision.
- Reusing design platforms provides market leverage over multiple product cycles.

Thus, there are two opposing issues you must consider when designing libraries: time to market and costs. Industry economics (related partially to the complex nature of manufacturing small geometry silicon and short product lives driven by consumers) have little room for political or technical arguments. Instead, the answer for many system providers is reusable design platforms. Some key advantages of design platforms are as follows:

- Allowing a provider to capture multiple market segments by amortizing large and growing design costs and reducing time to market.
- Reducing the number of core processor architectures, while allowing more differentiation at the software application level.
- Increasing the percentage of mixed-signal designs as high-speed and mobile applications are integrated into a single silicon system-on-chip (this does not need to be a SoC it could be a multi-die solution or even a small form factor by board implementation).
- Providing flexibility of outsourcing and integrating pre-verified intellectual property (IP) functional blocks.
- Increasing hardware and software programmability. For the system architects, the trade-off is hardware or software. Software offers flexibility but costs silicon real estate, degraded system performance, and increased power consumption.

- Enabling special emphasis or "special sauce" to be captured in custom blocks or in software.
- Including retargeted IP. Previously used IP substantially reduces functional risk.

12.3 HOW DID WE GET HERE, ANYWAY?

Electronic system design has evolved in the last 30 years into a hierarchical process, which generally can be separated into three groups: system design, hardware and software implementation, and manufacturing and test. Although each group has its own area of optimization, they each must maintain the design intent originally specified in the system requirements. Each level of the design hierarchy must preserve the design intent of the preceding level (Figure 12.1).

As the design progresses through the hierarchy, the details of design intent become more specific. Design intent at the system design level guarantees that the system performs the desired function under certain specifications, such as power and speed. At the hardware implementation level, design intent is preserved by block- and instance-level specifications. Finally, at the manufacturing level, design intent is preserved by the lowest-level primitives, such as transistors and metallization.

As an example, we can analyze the design of a cell phone.

The system supplier (e.g., Nokia) is typically the company that is familiar to the consumer. With an ever-increasing complexity in electronic systems, consumers have come to rely on a brand to make their purchase decisions. If all brands have equal qualities, the market becomes commoditized, and the only factor then is cost. For example, brands that command a premium price are Sony and Apple Computers. To avoid commoditization, system suppliers must continue to increase their systems' features and performance. Their tasks include market definition, product specification, brand identity, and distribution. The system designer in a company like Nokia works from a specification and describes the design in terms of behavior. The behavior can be expressed in a high-level language such as C, System C, or C++.

At hardware and software implementation, the implementation company (e.g., Texas Instruments) will create a logical and physical description. Brands in this area are less of a factor with the consumer (the notable exception being the lingo "Intel Inside," which managed to commoditize everyone else on the motherboard). The main concerns are design closure for performance, cost, and power. In the implementation phase, there must be a convergence of the design or closure. The litmus test for closure is whether the design has met the performance specifications in physical implementation.

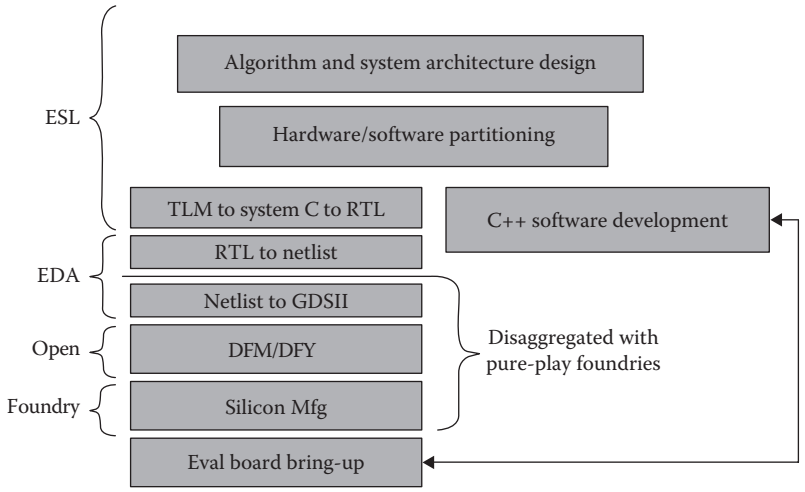

FIGURE 12.1 Design hierarchy.

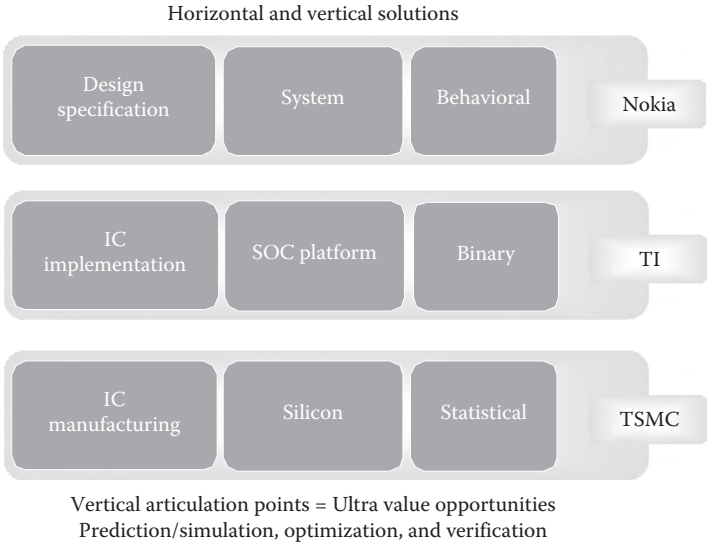

FIGURE 12.2 Horizontal and vertical design solutions for cell phone example.

At the manufacturing level, the manufacturing company (e.g., TSMC or Flextronics) provides manufacturing integration and test, process control, supply logistics, and capital utilization. In electronics design manufacturing, the measure of success is different from implementation. At the implementation phase, there is a binary decision (i.e., were the specifications met or not?). In manufacturing, it is statistical. Does the finished good fall in the statistical standard deviation that defines a good product?

In an increasingly disaggregated design chain, there must be efficient and accurate methods to communicate both vertically and horizontally to ensure the integrity of design intent. Figure 12.2 shows how horizontal and vertical solutions may appear for our cell phone example.

12.3.1 WHAT DEFINES HORIZONTAL DESIGN SPACE?

At any given step in the vertical hierarchy of the design process, there is a need to explore the design space. Engineers at each level must guarantee that the design intent from preceding levels is preserved. This entails understanding the design constraints, optimization of the design, and validation of the implementation at the current level.

Generally, the progression horizontally is the following:

- *Measure*: Using instruments automatic test equipment (ATE) or a computer program (timing analyzer) to measure the attributes of the current design.
- *Model*: A parameterized mathematical model of the behavior found through measurement, the accuracy of which is directly related to the level of statistical control. Typically, there is a trade-off between model accuracy and complexity. Often, developers look to develop the perfect model. This, in turn, drives more computation time and subsequently reduces the number of possible experiments due to limited resources. Generally speaking, there is more value in exploring a larger design space.
- *Analyze*: Tools to view and edit the results of the designer's experiments in optimizing the design against constraints.
- *Simulate*: An engine using the models defined in the lower levels of the design hierarchy to explore "what if" scenarios. This can expose more widely the opportunities to optimize.
- *Verify*: Often, the same engine is used in simulation, but with assertions on the design, to verify that design intent was not changed during design optimization.

- *Optimize*: A process that uses weighted design constraints to perform experiments to best fit the design. The optimization process can be performed using an automated or manual approach, depending upon the complexity of optimization and the number of experiments required. The drive is toward automation, but this is not always feasible.

Libraries in the horizontal solution will contain models, pre-verified IP, and a set of rules (test benches, design rules, or lower-level models) for verifying the design. A test bench implements an automated method for generating stimulus to apply to the model of the design, along with the means of comparing the expected results with the simulated results.

In terms of economic value, in the history of electronic design automation (EDA), more value has been awarded to simulation and optimization products that follow analysis in the horizontal flow. While modeling is a very difficult but necessary step, it has not been able to extract the same value.

12.3.2 WHAT IS A VERTICAL DESIGN SOLUTION?

In the vertical axis of the design chain, the critical step is verification of the design as it moves through the vertical design chain flow.

An excellent example is at the physical verification step, where you verify whether an IC design has met the manufacturer's rules. The best execution of verification is to use the same physical verification engine and rules that the manufacturing semiconductor foundry will use to verify the design for manufacturing. In the past, verification tests were based solely on geometric rules, but they now rely increasingly on a model-based approach to ensure manufacturability. It has become an extremely difficult problem to ensure that design intent is maintained, as the design moves from a binary to a statistical world. Several companies (e.g., ARM, Virage) have established an excellent business of developing standard physical library elements for pure-play foundries (e.g., UMC, TSMC) that already take into account the manufacturing variability bridging graphic data system II (GDSII) to silicon.

In another example, at the system level of the design chain, the software developer relies on hardware behavior models to optimize software application. In this area, the software engineer has no concept of a clock, as a hardware design would. The processor model only needs to be "cycle" accurate to ensure that the application can be verified effectively. Several companies (e.g., Virtutech, VAST, and Carbon) have offered their approach to modeling the processor behavior.

12.4 COMMERCIAL EFFORTS

These examples have illustrated that there is a need for IP or libraries in both the horizontal and vertical design chain. This need was recognized far back in the early 1970s. Early efforts such as in [1,2] concentrated on supplying the physical design of standard cells. Then new forms of modeling were added, typically behavioral and timing [3]. Integrated design and manufacturing houses explicitly built libraries to ease vertical integration [4], and vertically integrated systems implicitly included libraries [5,6]. As processes became more complex, libraries were also characterized for faults [7], signal integrity [8], and yield [9]. There are now companies such as ARM [10] and websites such as Design and Reuse [11], which are completely devoted to IP and libraries.

Economically, the commercial efforts that have done well have developed a *de facto* standard for communicating design intent across the design chain. The design chain adopts them as the standard protocol to communicate design data. They have enjoyed a proprietary position through a combination of business models and technologies, enabling them to establish broader product and service portfolios. Examples are Synopsys with their DesignWare and timing libraries, Rambus with memory controllers, Artisan with standard cells and memories, and Meta Software with SPICE models.

It is interesting that the market capitalization for the major IP companies has grown significantly (e.g., ARM, RAMBUS, Tessera, and Synopsys with DesignWare). These commercial IP companies have been able to capture significant value from the design chain, as it has become disaggregated. What is different with regard to the traditional EDA companies is that once IP is established, there is room for only one dominant supplier. As the design chain disaggregates, the requirements of preserving design intent create high-value opportunities (i.e., pre-verified IP, EDA tools, or semiconductor manufacturing). In the physical IP space, the use of the IP can insulate the designer from the changing physics of manufacturing, so the designer can focus on creating value in the design, and not on whether manufacturing can deliver the design intent. The details are embedded in the physical IP.

IP will continue to increase in value, as the design chain continues to disaggregate, and the difficulty of communicating design intent increases. For example, the complexities of manufacturing, both in the physics (lithography, etch, and CMP) and in logistics (global supply chains), require efficient and accurate virtual use of information by teams that know no political or time boundaries. The winners will solve not only the modeling problem technically but also the business challenges of addressing this 24/7/365 world.

There will be growth in the IP and libraries in the horizontal domain as current EDA models continue to mature. We can think of it in terms of an "evolution" that will identify more parameters (e.g., 48 term BSIM4 SPICE models that now include power), new analysis technologies (software and hardware) for dealing with the increased compute and data volumes, and new assertion cases for verification.

12.5 WHAT MAKES THE EFFORT EASIER?

IP and library standardization of information would be a great step forward. Standardization is usually the instrument of market expansion. Common interfaces between vertical domains allow the free and unencumbered exchange of information.

12.6 ENEMIES OF PROGRESS

The design solutions that made winners in the past will not work with the speed of the market today. The following is a list of issues that have caused problems in the past, especially in IP and libraries. These should be avoided if possible:

- Warring tribes that miss the "Big Picture" of consumer demands (UNIX vs. DEC/VMS; VHSIC Hardware Description Language vs. Verilog; System Verilog vs. SystemC, etc.).
- Unclear benefits such as the supplier controlling the agenda.
- Companies holding onto proprietary formats, until it becomes detrimental to their growth. Some enlightened suppliers have seen the future and have opened their standards.
- Political motivation that limits competition (DivX and IBM Microchannel).
- Customer edict without sufficient vendor input (e.g., OLA, another logical format [ALF], VHDL, Wal-Mart, and radio frequency identification [RFID]).
- Difficult to adopt and no mapping of existing infrastructure. No one has the time or money to do something that does not have a clear and efficient cost/benefit over existing solutions.
- The installed base is incompatible, and the cost to adopt is prohibitive.
- Standards that are ahead of their time, and solutions looking for problems.
- Perfection can be the enemy of a good solution. Good enough will win the day. Do not postpone for perfection.
- Abstraction without effective automation. This is generally a gap between domains that are not interconnected. As a result, the standard becomes useless.

12.7 ENVIRONMENTS THAT DRIVE PROGRESS

There are circumstances that make IP less of a limiting factor and more of an enabler. In order to increase system complexity and continue manufacturing that enables differing versions of IP, you need to consider the following attributes:

- Design is increasingly driven by cost, efficiency, and functionality over raw performance. Does the world need any more MIPS?
- The effective communication of design intent and the use of models to the surrounding levels in the design chain.
- Cost pressures will cause industry consolidation around new market aggregation layers (IP and library companies have and will continue to capture value). Other companies like eSilicon and OpenASIC are successfully using design and logistics information to develop new business models.
- Reliance on standards will amortize the cost by members of standard conforming groups.
- Open IP standards are allowing for a new road map of requirements and the development of commercial offerings (PCI-X, DDR1/2). Systems companies will innovate in the applications not in the protocols.
- Standards (products, architectures, interfaces, and abstractions) enable economies of scale and the reuse of platforms over multiple product cycles.

12.8 LIBRARIES AND WHAT THEY CONTAIN

The following lists are examples of libraries at various levels in the vertical design hierarchy (from low to high) as well as the methods for communication:

12.8.1 LOW-LEVEL PHYSICAL IP

- These include standard cells, memory, analog/mixed signal IP, and interface IP, such as I/O cells and PHYs. (PHY is a generic term referring to a special electronic circuit or functional block of a circuit, which provides physical access to a digital interconnect cable.)
- Examples: ARM Holdings, Virage, internal design groups, etc.
- Typical libraries enable variations to optimize area, speed power, and increase the yield. These are implemented via configuration or cell variants.
- Outputs to higher levels in the design hierarchy: cell layout (typically GDS-II), routing model (typically LEF), functional models (typically Verilog), timing models (typically. lib), circuit models (typically SPICE), and yield models (often PDF solutions format).
- Inputs from lower levels in the design hierarchy (manufacturing): geometric rules, transistor device models, and yield trade-off rules.

12.8.2 HIGH-LEVEL PHYSICAL IP (CORES)

- Examples: ARM, MIPS, and OAK.
- Typical libraries offer time to market advantages with a functional and performance guarantee. Offer no aspect ratio control or functional flexibility.
- Outputs to higher levels in the design hierarchy: cell layout, routing model (abstract), functional model, timing model, and yield model.
- Inputs from lower levels in the design hierarchy: process models, lower-level IP models, and system specification.

12.8.3 HIGH-LEVEL SOFT IP

- Examples: serial bus controllers, processor cores.
- Advantages: flexible aspect ratio and usable with many processes.
- Disadvantages: may be difficult to communicate design intent to the physical implementer, complex soft IP may diminish due to complexities introduced in the manufacturing process. It is hard to provide a performance guarantee, since detailed implementation is unknown at design time.
- Inputs from higher levels in the design hierarchy: block-level specifications for performance and functionality.
- Outputs to lower levels in the design hierarchy: logic net list, performance parameters, and placement information.

12.8.4 SYSTEM DESIGN/IMPLEMENTATION

- Inputs from higher levels in the design hierarchy: high-level C code and system specifications.
- Inputs from lower levels in the design hierarchy: low-level models for function, timing, power, and area.
- Outputs to lower levels in the design hierarchy: block-level specifications and overall system specifications for performance and cost.

12.8.5 SYSTEM ARCHITECTURE

- System specification: market-driven specification starts the design process.
- Outputs to lower levels in the design hierarchy: system functional code communicates system functionality along with the system performance requirements to the system design phase.

12.9 UPDATE: LITHOGRAPHY LIMITS, NEW TRANSISTORS, AND IMPLICATIONS FOR LIBRARIES

At technology nodes with feature sizes below 40 nm, library design necessitates a much more intimate interaction between the manufacturing process engineers and the design engineers. This is due to the fact that advances in lithography have plateaued in terms of resolution with 193 nm light sources in immersion-based scanners. This has imposed new constraints on library designers, particularly in the physical implementation and layout of library elements.

In addition, new transistor structures like FinFETs will have a significant impact on library architectures, circuit design, and modeling.

12.9.1 193 NM IMMERSION LITHOGRAPHY

The minimum feature size of an optical system is directly proportional to the wavelength of light and inversely proportional to the numerical aperture (NA) of the optical system. Light sources have reached a limit of 193 nm (deep ultraviolet excimer laser). Light sources of 193 nm were first widely deployed at the 65 nm node. The next advance in shorter wavelength light sources has been focused on extreme ultraviolet (EUV) with wavelengths of 13.5 nm. EUV is still in development, facing a number of technical challenges to see wide-scale deployment.

With wavelengths being limited to 193 nm, improvements in numerical aperture have been made using water instead of air as the interface. Water's refractive index allows an increase to a NA of 1.35 from 0.93 in today's immersion lithography systems. Immersion lithography was first deployed at 45 nm and will be the workhorse system down through at least the 14 nm node.

12.9.2 DESIGN PROCESS CO-OPTIMIZATION

With both wavelength and NA having plateaued, another variable that can help improve the resolution of smaller feature sizes is controlling the complexity of the patterns that are required to be printed. Complex patterns with bends and jogs in close proximity to each other are difficult to resolve and set up interference patterns that are unpredictable. In more advanced technologies, standard cell designers have to deal with proximity effects. This entails placing a cell surrounded by representative neighboring cells and extracting the parametric variations due to these neighboring cells. These variations are then factored into the electrical characterization of the cells. In addition, design margins for variability on a broader scale across the entire chip must be factored in with OCV (on chip variability) factors.

The easiest pattern for an optical system to resolve is a series of straight lines on a fixed pitch. Since transistor variation is a critical concern, manufacturers have begun requiring restrictions at the 32/28 nm node on the gate-level layout that essentially results in the gate layer being a series of straight-line patterns. This restriction forces cell library designers to develop alternative cell architectures and physical implementation methodologies.

In advanced technology nodes, the limits of optical lithography in terms of process variability and design rule restrictions are driving a much closer collaboration between library designers and the process development community. This collaboration must not only be close but must start much earlier in the design of a new node, as trade-offs between the manufacturing process and its impact on design must be rationalized early in the development cycle. From an industry standpoint, this has led manufactures, including "pure-play" foundries, to invest in library designs teams while at the same time forging closer alliances with customer library teams as well as third-party library entities.

12.9.3 BEYOND THE RESOLUTION LIMIT

Even straight-line patterns run into resolution issues at feature sizes associated with the 20 nm node. In the absence of shorter wavelength lithography like EUV, the techniques associated with double patterning or multiple patterning are the only solution available. A simplistic illustration of double patterning for a series of straight lines would be creating two lower resolution masks, with alternate lines on each mask. This shifts the lithography challenge from resolution to alignment accuracy, as the second pass line patterns must be accurately interleaved with the first pattern in order to achieve accurate spacing between all the lines. There are many techniques in the industry to accomplish this type of resolution improvement.

Some involve multiple optical exposures, and others use a single exposure and multiple process steps to implement a technique referred to as pitch division to increase resolution. In general, the impact on cell library designers involves restrictions on layout rules to enable these multi-patterning approaches to be implemented.

The combination of layout restrictions for variability and multi-patterning is driving the EDA (Electronic Design Automation) industry to also collaborate more closely, and early, in the process development phase. The complexity of dealing with these restrictions and their interactions must be automated, in order to be feasible to implement the billion transistor designs that 28 and 20 nm nodes enable. Additional complexities introduced by new transistor structures will put additional burdens on EDA companies to help automate and model the interactions of these new technologies.

12.9.4 NEW TRANSISTORS

At 20 nm and below, companies are beginning to deploy new transistor structures, in particular FinFET or 3D Tri-Gate, that have very fundamental design differences and implications for cell library design. These transistor structures have dramatically improved power-performance characteristics and are hence attractive for all applications, in particular for the proliferation of battery-operated mobile devices [12].

The discrete size of the fin in these devices leads to a quantization in terms of transistor sizing. The width of the transistor is no longer a continuum but a multiple of the number of fins. This is a significant change that standard cell library designers must deal with, in architecting the overall library or family of libraries, in terms of area, performance, and power. Another key issue for FinFETs is the 3D nature of the structure and the complex modeling implications of this [13]. As these devices are new, many of the design rules and models remain proprietary and in some cases are still preliminary depending upon the manufacturer. Cell library innovation using FinFETs is currently an active industry topic and opportunity for differentiation in the industry.

12.10 SUMMARY

Standard cell-based designs remain the dominant approach for the implementation of SoC, ASICs being deployed in the vast majority of today's consumer, communications, and computer products. Libraries must be deployed in advance of the time that leading edge processes are brought on line, in order for designers to have products taping out to fill the massive fabs brought online in support of these high-volume consumer applications. In parallel, the EDA industry is grappling with many simultaneous technical challenges. They include

- Increasing product complexity, the drive to improve design productivity and shorten design cycles
- Increasing the complexity of manufacturing processes, forcing the knowledge of manufacturing physics up the design hierarchy to cause multiple non-convergent optimization problems (Litho and DFM/DFY)
- Critically verifying and solving the equivalence problem of design intent
- Increasing need for a higher level of design abstraction/handoff to foster more design starts
- Optimizing multiple simultaneous design objectives, including power, timing, signal integrity, etc.

The market has matured—the EDA standards process must also rise to a new level. This will include IP as well as tools in their design solutions. IP and library products that address the stated challenges by bridging the horizontal and vertical design chain articulation points are and will be more valuable. New process technologies require library designers to have not only an in-depth knowledge of circuit design but also a broad knowledge of adjacent technology considerations in terms of device design and process development. Close collaboration among companies and entities in manufacturing, library design, chip design, and EDA is essential for success in advanced technology nodes.

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