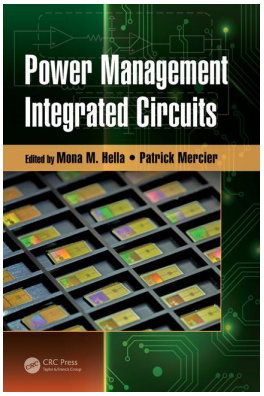

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3 SIMO Power Converters with Adaptive PCCM Operation

Yi Zhang and D. Brian Ma

CONTENTS

3.1 BACKGROUND AND MOTIVATION

Driven by modern very large scale integration (VLSI) systems and their fast-emerging applications, the demands on multiple on-chip power supplies have been ever increasing due to two main reasons. First, as complexity of electronic devices such as cell phones and laptops increases, multiple power supplies are essential to power key functional blocks, such as processors, liquid crystal display, and radio transceivers. Second, as power consumption in semiconductor chips rises, efficient system power management techniques are in high demand. This leads to the high popularity of the so-called dynamic voltage/frequency scaling (DVFS) techniques (Burd et al. 2000, Chang and Pedram 1997, Cheng and Baas 2008, Ma and Bondade 2010, Usami et al., 1998),

where multiple-supply-based power management schemes are crucial. By powering distinct functional modules and subsystems with different supply voltages and by adaptively switching their supplies according to instantaneous power needs, power and energy savings achieved through DVFS techniques are significant (Burd et al. 2000, Luo et al. 2007, Ma and Bondade 2010).

Historically, multiple DC power supplies are implemented by transformer-based isolated DC–DC converters or several nonisolated DC–DC converters. However, due to the use of bulky off-chip inductive components and many power switches, system volume, printed circuit board (PCB) footprint, and electromagnetic interference noise are all considerably large. In the meantime, regulation accuracy can be compromised by commonly used "master–slave" regulation approaches (Ma et al. 2001a).

To mitigate these issues, single-inductor multiple-output (SIMO) power converters were proposed (Ki and Ma 2001, Ma et al. 2001a, 2003a,b). By time-sharing a single inductor and some power switches, a SIMO power converter offers multiple power outputs, which can be regulated independently. This leads to a significant reduction in cost, volume, and PCB footprint. Because of their cost-effective features, the application of SIMO power converters has been proliferating in recent years, spanning from hybrid power source units (Huang et al. 2010), energy-harvesting systems (Kim and Rincon-Mora 2009, Sze et al. 2008) to light-emitting diode backlighting (Chen et al. 2012), active matrix OLED display panels (Chae et al. 2009), and electronic paper displays (Lee et al. 2010).

As more SIMO converter-based IC products are being commercialized in the market, cross-regulation effect, as one of the most critical design challenges, has drawn extensive attention. In a SIMO switching converter, because the inductor is time-shared by several subconverters, a duty ratio change in one subconverter may affect the amount of energy transferred to other subconverters even if the operating conditions (load currents, duty ratios, etc.) in other subconverters remain constant. As a result, this may cause voltage variations on the affected outputs. This effect was named as cross-regulation in Ma et al. (2003b) because a local operating condition change in one subconverter has impacted the regulation performances across the others. In worst-case scenarios, a SIMO converter fails to operate due to severe cross-regulation.

In order to avoid the cross-regulation effect, the regulation time slot designated to each subconverter should be completely isolated. For this reason, SIMO converters in the early stage usually operate in discontinuous conduction mode (DCM) (Ki and Ma 2001, Ma et al. 2001a, 2003b). However, in heavy-load scenarios, peak inductor current may rise very high in DCM, causing substantial voltage and current ripples and switching noise. Alternatively, if continuous conduction mode (CCM) is applied to alleviate large peak current, cross-regulation occurs immediately. In order to reduce the heavy current stress while retaining low cross-regulation, a pseudo-continuous conduction mode (PCCM) operation was first proposed in Ma et al. (2002). Instead of returning to zero as in DCM, the inductor current stays constant at a predefined current level through freewheel switching actions. With the same load condition, the peak inductor current in PCCM can be much lower than that in DCM, while still avoiding cross-regulation effect since the regulation actions on any two

outputs are isolated by one freewheel switching period. Unfortunately, the PCCM operation also has its own drawbacks. Especially, in the unbalanced load conditions, large conduction power loss is observed in subconverters handling light loads. Moreover, since the freewheel switch turns on/off multiple times in one switching cycle, the overall switching power loss also increases. To overcome these drawbacks, a new control technique is required to reduce both conduction and switching power loss in the freewheel switch.

3.2 DEVELOPMENT OF SIMO POWER CONVERTERS

To better understand the PCCM operation for SIMO converters, we first examine the development of SIMO power converter, as illustrated in Figure 3.1 (Ma et al. 2001a, 2003b). Consider two conventional switching boost converters in DCM operating at the same switching frequency. One possible operation scheme is illustrated in Figure 3.1a. At the beginning of each switching cycle T, the inductor L_1 is charged at a rate of V_{IN}/L_1 until $D_{11}T$ expires, where D_{11} is the duty ratio of the switching power converter 1. During $D_{21}T$, the inductor L_1 is discharged at a rate of $-(V_{IN} - V_{O1})/L_1$ and

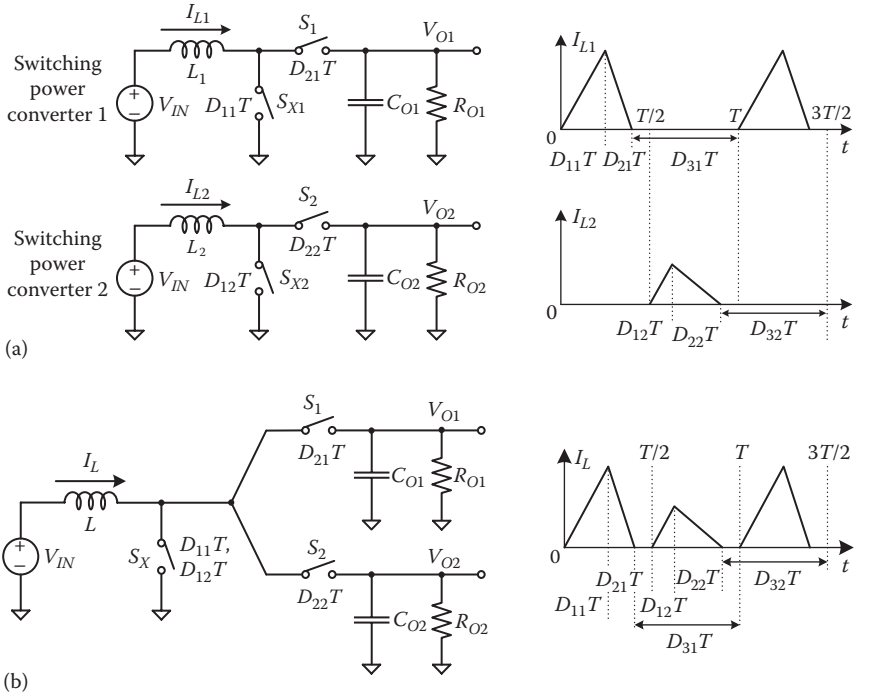

FIGURE 3.1 Power stage architecture and discontinuous conduction mode inductor currents of (a) two conventional switching power converters and (b) one single-inductor multiple-output converter. (From Zhang, Y., Single-inductor multiple-output power converters: Architectures, control techniques and applications, PhD dissertation, The University of Texas at Dallas, Richardson, TX, 2013.)

I_{L1} drops down until it returns to zero. The inductor current stays at zero during $D_{31}T$. Similar operation scheme applies to the switching power converter 2.

If the two inductor currents can be alternately assigned to occupy different parts of the switching cycle without overlapping, only one single inductor will suffice for their operation, as shown in Figure 3.1b. During the first half switching cycle from 0 to $T/2$, the inductor current is diverted to V_{O1} by properly controlling the power switches S_X and S_1. Similarly, in the second half switching cycle, S_X and S_2 are turned on/off to deliver the inductor current to V_{O2}. With this method, the inductor L is shared by the two subconverters in a time-multiplexing manner. Hence, a SIMO power converter with a time-multiplexing operation scheme is developed.

Obviously, this operation scheme can be readily extended for SIMO power converters with more than two outputs. For SIMO power converters with N subconverters, one switching cycle is divided into N phases, with the inductor current being multiplexed into each output during the corresponding phase. Furthermore, the topology is not only limited to boost converter. It can be easily extended to many existing switching power converter topologies (Ki and Ma 2001), such as buck and noninverting buck–boost.

It should be noted that the time-multiplexing operation is critical for a SIMO power converter. The inductor current is assigned to each subconverter alternately. Each output only occupies its own phase in one switching cycle. These phases are expected to be isolated in order to prevent cross-regulation. When the inductor current is being diverted into one subconverter, the other one is separated from the control loop. In other words, only one switching subconverter is being regulated at a time instant.

3.3 PRIMARY TOPOLOGIES

Similar to the conventional single-output switching power converters, the SIMO power converters can also be categorized into different types based on the topologies. In this section, the three primary topologies for SIMO power converters—boost, buck, and noninverting buck–boost topologies—are introduced.

3.3.1 Boost Topology

The power stage architecture and timing diagram of a SIMO boost switching converter with two outputs are illustrated in Figure 3.2. The two subconverters are regulated by a pair of complementary clocks Φ_1 and Φ_2, with power delivered to each output from the supply V_{IN} in a time-multiplexed manner. The working principle can be described with reference to the timing diagram illustrated in Figure 3.2b. When the first subconverter is operating, $\Phi_1 = 1$ and the switch S_2 is off. No current flows into the output V_{O2}. Meanwhile, S_X is on. The voltage across the inductor is, thus, the supply voltage V_{IN}. The inductor current I_L increases during $D_{11}T$:

$$\frac{di_L}{dt} = \frac{V_{IN}}{L}. \tag{3.1}$$

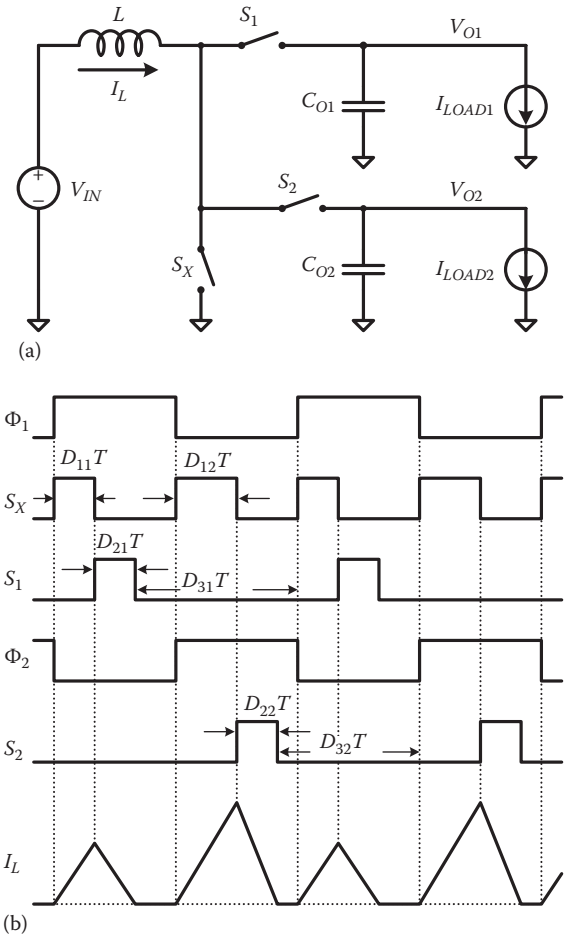

FIGURE 3.2 (a) Power stage architecture and (b) timing diagram of single-inductor multiple-output boost converter.

During $D_{21}T$, the switch S_X is off and S_1 is on, causing the inductor to discharge the current into the output V_{O1}. The slope of the inductor current is given by

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{O1}}{L}. \tag{3.2}$$

As the output voltage of a boost converter is greater than the supply voltage, the rate of the inductor current change is negative. As illustrated in Figure 3.2b, the inductor current decreases and delivers the required charge to the output. When it goes to zero, the converter enters $D_{31}T$ and the switch S_1 is turned off. The inductor current

stays at zero until the phase Φ_2 begins. Hence, the duty ratios D_{11}, D_{21}, and D_{31} satisfy the requirements shown as follows:

$$D_{11} + D_{21} \leq \frac{1}{2}, \tag{3.3}$$

$$D_{11} + D_{21} + D_{31} = 1. \tag{3.4}$$

During $\Phi_2 = 1$, the inductor current is multiplexed into the output V_{O2} and similar switching actions repeat for the subconverter 2. With this method, the two outputs are regulated in a time-multiplexing manner by sharing the inductor L and the power switch S_X. Compared with two traditional switching boost converters, the number of off-chip magnetic component and power switches is both reduced. Obviously, with the increase of the number of subconverters, this cost reduction effect will become more significant.

3.3.2 Buck Topology

Another primary type of SIMO power converters are constructed with buck topology. Figure 3.3a shows the power stage architecture of a SIMO buck power converter with two outputs. The power stage consists of one inductor L; four power switches S_P, S_N, S_1, and S_2; and two filtering capacitors C_{O1} and C_{O2}. The two subconverters share the inductor L and power switches S_P and S_N. The timing diagram of DCM operation is illustrated in Figure 3.3b. Similar to the boost SIMO converter, the two subconverters are regulated alternately during Φ_1 and Φ_2. The two output voltages are stabilized at lower voltage levels than the input voltage, thereby achieving step-down DC–DC voltage conversions. The inductor current slope during charge and discharge periods is defined by

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{Oi}}{L}, \tag{3.5}$$

$$\frac{di_L}{dt} = -\frac{V_{Oi}}{L}, \tag{3.6}$$

where i equals 1 or 2. Compared with two traditional buck converters, the number of inductors being used is halved. Although the number of power switches is not reduced, the cost effectiveness can still be observed when more subconverters are incorporated.

3.3.3 Noninverting Buck–Boost Topology

The third type of topology for SIMO power converters is noninverting buck–boost topology, which achieves both step-up and step-down voltage conversions. As shown in Figure 3.4a, the two subconverters share the inductor L and power switches

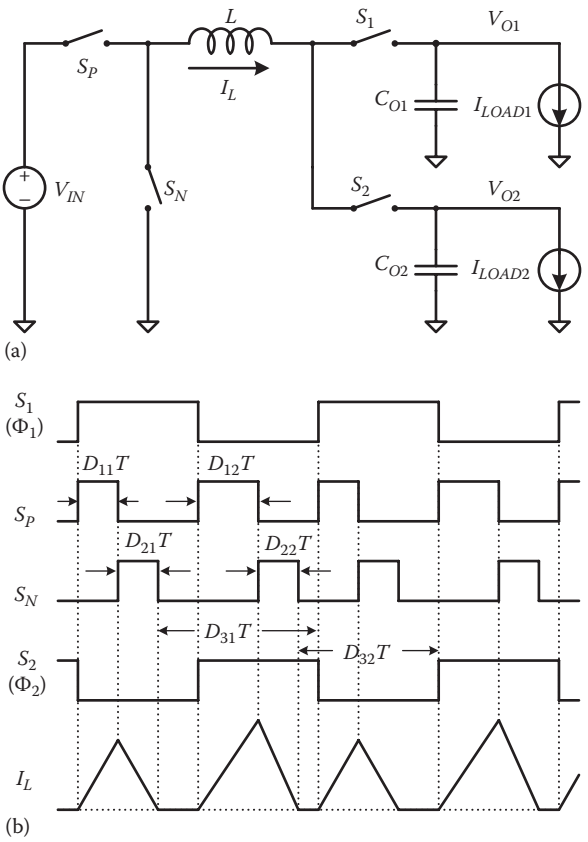

FIGURE 3.3 (a) Power stage architecture and (b) timing diagram of single-inductor multiple-output buck converter.

S_P, S_N, and S_X. The corresponding timing diagram is demonstrated in Figure 3.4b. In each phase, during the charge period, S_P and S_X are enabled, thereby charging up the inductor with a slope of V_{IN}/L. Similarly, during the discharge phase, S_N and S_i are turned on. The inductor current ramps down with a slope of $-V_{Oi}/L$ (i = 1 or 2). Compared with the boost and buck topologies, the noninverting buck–boost topology demonstrates higher flexibility regarding the voltage conversion ratios. The output voltage can be stabilized at higher, lower, or similar voltage levels compared with the input voltage. However, this flexibility is achieved at the cost of more power switches. The corresponding switching power loss and control complexity for noninverting buck–boost topology are, thus, increased compared with the other two topologies.

In addition to these three topologies, there are also other topologies that can be used in SIMO power converters. For example, inverting buck–boost topology allows the generation of negative output voltages. When combined with the aforementioned topologies, both positive and negative output voltages can be implemented.

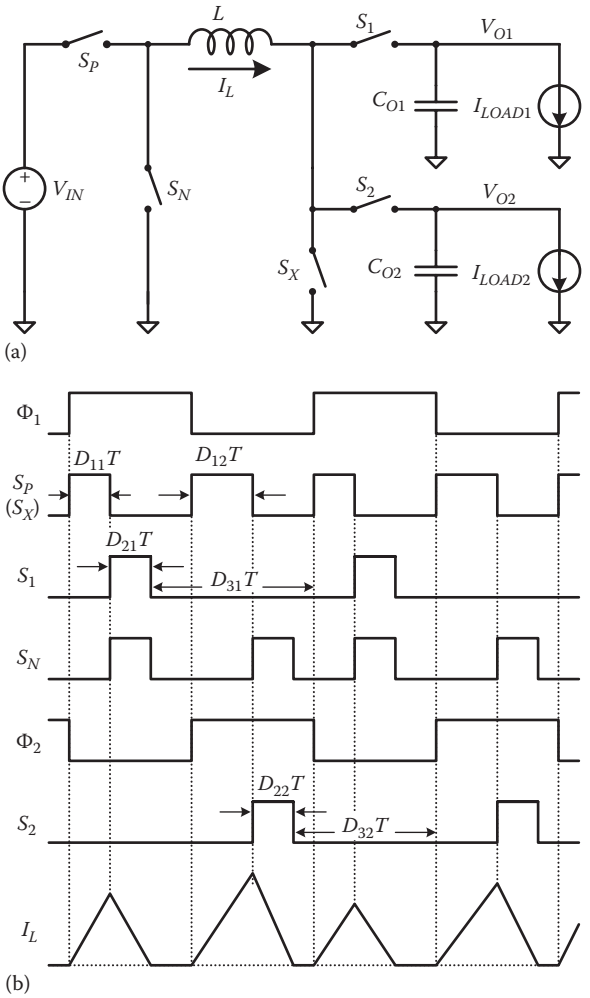

FIGURE 3.4 (a) Power stage architecture and (b) timing diagram of single-inductor multiple-output noninverting buck–boost converter.

As a result, it leads to SIMO converters with bipolar power outputs (Ki and Ma 2001, Ma et al. 2001b).

3.4 CONVENTIONAL OPERATION MODES

Historically, based on the inductor current, the operation mode for SIMO power converters can be categorized into two types: DCM (Ki and Ma 2001, Ma et al. 2001a, 2003b, Sze et al. 2008) and CCM (Belloni et al. 2008, Goder and Santo 1997, Li 2000, May et al. 2001). This section addresses both in due course, using a single-inductor dual-output (SIDO) boost topology as an example.

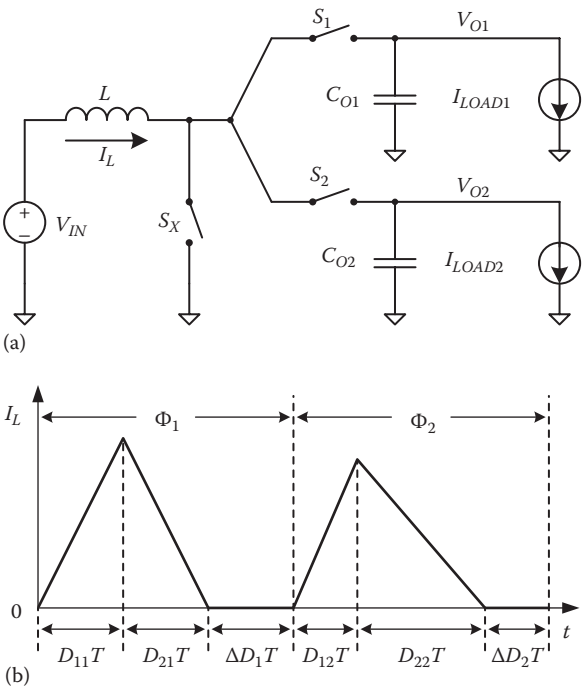

FIGURE 3.5 (a) Power stage architecture and (b) inductor current waveform of a single-inductor multiple-output boost converter operating in discontinuous conduction mode.

3.4.1 Discontinuous Conduction Mode

The typical inductor current waveform in DCM operation is shown in Figure 3.5. At the beginning of each phase, the inductor is charged. The charge process ends when $D_{1i}T$ expires, followed by a discharge period. Instead of occupying the rest of the phase, the discharge period, $D_{2i}T$, ends once the inductor current drops to zero. After it, the inductor current stays at zero until the next phase is enabled. Since each subconverter only operates within its own phase, no two adjacent phases are overlapped, thereby eliminating the potential cross-regulation effect.

3.4.2 Continuous Conduction Mode

While the DCM operation can effectively suppress cross-regulation, it has certain drawbacks at heavy load conditions. With the same input/output voltages and load current, in order to deliver the same amount of charge with the same switching frequency, the peak inductor current value in DCM operation is usually much higher than in CCM. Hence, under heavy load conditions, DCM operation leads to large voltage/current ripples and switching noise.

Alternatively, another operation mode for SIMO power converters is CCM. As shown in Figure 3.6, the inductor is charged from the beginning of each phase.

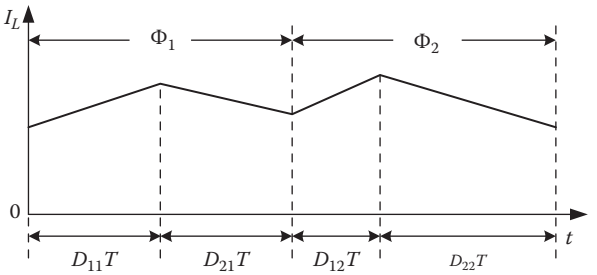

FIGURE 3.6 Inductor current waveform of continuous conduction mode operation.

This charge process continues until the time period $D_{1i}T$ expires, where i equals 1 or 2. Then, the discharge period $D_{2i}T$ is enabled until the discharge phase ends. The inductor current charge and discharge actions are repeated in each phase, thereby delivering the desired power from input to the corresponding output. Since the next phase starts immediately after the current phase expires, the inductor current is kept continuous during the phase transition periods. Such type of operation scheme is thus called CCM.

Due to the continuous conduction property, the inductor current is always maintained above zero. As a result, compared to the DCM operation, the CCM operation facilitates lower inductor current ripples, which in turn reduces output voltage ripples. Moreover, since the inductor current never goes to zero in CCM, the potential negative/reverse inductor current, which may occur in DCM operations, is avoided, thereby improving the power efficiency. From the circuit design perspective, the zero current detector and active diodes can be obviated. The circuit complexity and design challenge are both reduced.

However, CCM operation also incurs some drawbacks. Due to the continuous conduction property, the inductor current at the end of each phase is uncertain. As a result, the initial value of the inductor current to the second subconverter is dependent to the end value of the first one. If a sudden load change occurs in one phase, it will inevitably affect the subsequent phases, causing severe cross-regulation problems (Ma et al. 2003b).

3.5 PSEUDO-CONTINUOUS CONDUCTION MODE

In order to receive the benefits from both CCM and DCM operation schemes, the PCCM was proposed for SIMO power converters (Ma et al. 2002, 2003a). In the PCCM mode, as depicted in Figure 3.7 and similar to a CCM one, the inductor current of a SIMO converter always stays greater than a predetermined DC value I_{dc}, thus reducing the inductor current ripples. This is achieved by shorting the inductor with the aid of a freewheel switch S_{fw} while keeping the other switches off. With reference to Figure 3.7, when Φ_1 is enabled and during the period $D_{21}T$, when the value of the inductor current reaches I_{dc}, S_{fw} is turned on and all the other switches are turned off until Φ_1 expires. This period is known as the freewheel switching period.

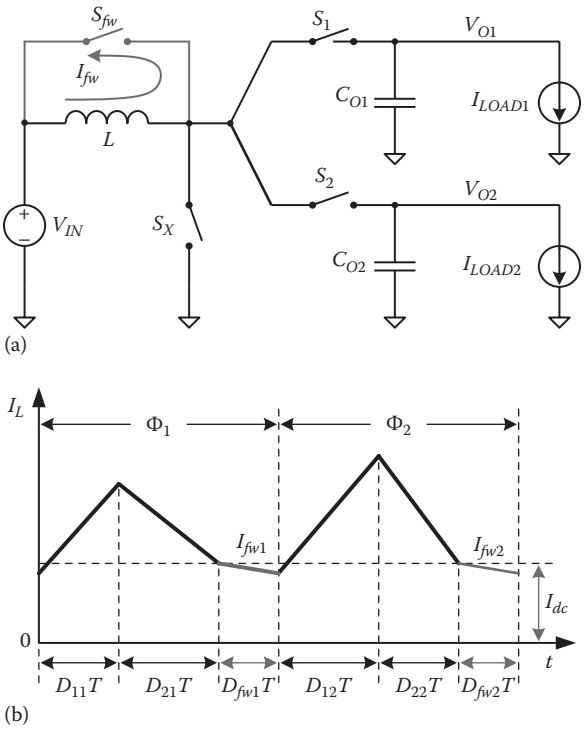

FIGURE 3.7 (a) Power stage architecture and (b) inductor current waveform of a single-inductor dual-output boost converter operating in pseudo-continuous conduction mode.

A similar period occurs during Φ_2. As the current continuously stays above I_{dc}, it allows the converter to handle heavy current loads with low ripples. Moreover, since the two subconverters are isolated by the freewheel switching periods, cross-regulation is also avoided.

Despite the aforementioned advantages of PCCM operation, there remain some drawbacks. To avoid cross-regulation, the freewheel switching current level I_{dc} has to be chosen to satisfy the largest load current among all the outputs. If the value of I_{dc} is reduced, then a load change at either output could cause one of the subconverters to enter the CCM mode. For example, assume I_{LOAD1} suddenly increases. The inductor has to be energized to a larger current value in Φ_1 to satisfy the higher power demand. I_L, thus, may not be able to return to I_{dc} before Φ_1 expires. The converter then enters the CCM mode. Meanwhile, if the freewheel switching period $D_{fw}T$ is too long, the turn-on resistance of the freewheel switch and the direct current resistance (DCR) of the inductor can cause significant conduction loss. This is especially pronounced during unbalanced load conditions, as shown in Figure 3.8, in which a long $D_{fw}T$ can be observed in the light-load subconverter. Moreover, the switching power loss of S_{fw} also becomes significant when the number of subconverters is increased.

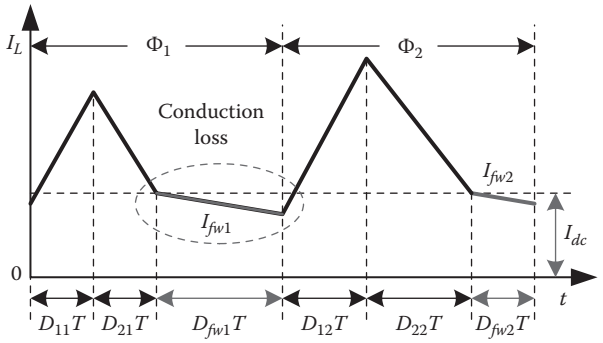

FIGURE 3.8 I_L during pseudo-continuous conduction mode operation in unbalanced load condition.

3.6 ADAPTIVE PCCM OPERATION

To resolve the problems of traditional PCCM, adaptive PCCM operation schemes are developed (Zhang and Ma 2010, 2011, 2012b, Zheng et al. 2010). By adaptively adjusting the freewheel switching durations and the freewheel current level I_{dc}, conduction power loss can be significantly reduced. Moreover, by switching S_{fw} only once per switching cycle, the switching power loss due to S_{fw} is also reduced. Since all the subconverters are still operating in PCCM, low cross-regulation can still be achieved.

3.6.1 Power Loss Analysis

Figure 3.9a models a freewheel switching loop. The resistance of the freewheel switch, R_{ON}, and the DCR of the inductor, R_L, both contribute to conduction power loss. To simplify the analysis, the sum of R_{ON} and R_L is named as R_{EQ}. Due to the voltage drop across R_{EQ}, I_L during the freewheel switching period $D_{fwi}T$ (i = 1 or 2) decreases gradually as in Figure 3.9b. I_L is, thus, given as

$$I_L(t)=\begin{cases} I_{dc}\cdot e^{-\frac{R_{EQ}}{L}[t-(D_{11}+D_{21})\cdot T]} & (D_{11}+D_{21})\cdot T\le t\le \dfrac{T}{2}, \\ I_{dc}\cdot e^{-\frac{R_{EQ}}{L}\left[t-\left(\frac{1}{2}+D_{12}+D_{22}\right)\cdot T\right]} & \left(\dfrac{1}{2}+D_{11}+D_{21}\right)\cdot T\le t\le T \end{cases}. \tag{3.7}$$

Consequently, the conduction power loss by S_{fw} is derived as

$$P_C=\sum_{i=1}^{n}\frac{I_{dc}^2 L}{2T}\left(1-e^{-\frac{2R_{EQ}}{L}\cdot D_{fwi}T}\right), \tag{3.8}$$

which reveals that the loss is highly related to I_{dc} and the freewheel switching period.

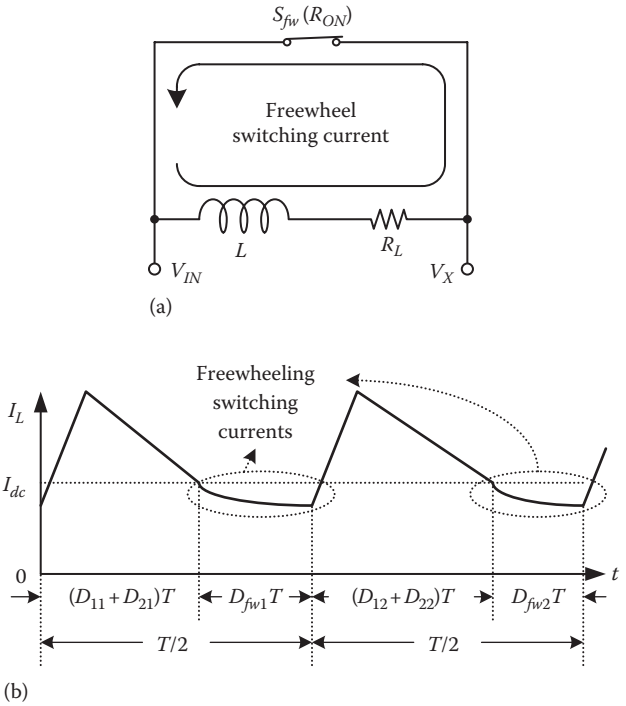

FIGURE 3.9 (a) Circuit model and (b) the inductor current waveform of the freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

In addition to the conduction loss, a freewheel switch induces two types of switching losses: the *V–I* overlap power loss and the gate-drive power loss. The cause of *V–I* overlap power loss is illustrated in Figure 3.10b. Due to the parasitic capacitors (C_{GD} and C_{GS} in Figure 3.10a), the gate voltage V_{gate} of S_{fw} cannot step up/down abruptly, leading to the overlapping periods between nonzero voltage V_{SD} and nonzero current I_D. The converter loses power during such *V–I* overlapping transient periods. Meanwhile, as shown in Figure 3.10b, before/after the turn-on/turnoff events, a dead time is usually added to avoid shoot-through current. During such a dead time, all the power transistors are turned off and the inductor current flows through the body diode of S_{fw}. As a floating switch, S_{fw} is usually implemented with a PMOS power switch. The substrate of the PMOS switch S_{fw} is usually tied to the highest voltage in the system ($V_{\max}$), which is one of the output voltages in a SIMO boost converter (Ma 2007, Zhang and Ma 2012a, Zheng and Ma 2011). If the voltage drop across the body diode is neglected, V_{SD} in S_{fw} swings between ($V_{\max} - V_{IN}$) and ground. The turn-on process starts at t_1 by discharging the gate capacitance. When the gate voltage drops to $V_{\max} - V_T$ at t_2, S_{fw} starts to conduct current. When I_D increases from zero to the full freewheel switching current I_{dc} at t_3, V_{SD} starts to be pulled down. This continues until V_{SD} drops to zero at t_4.

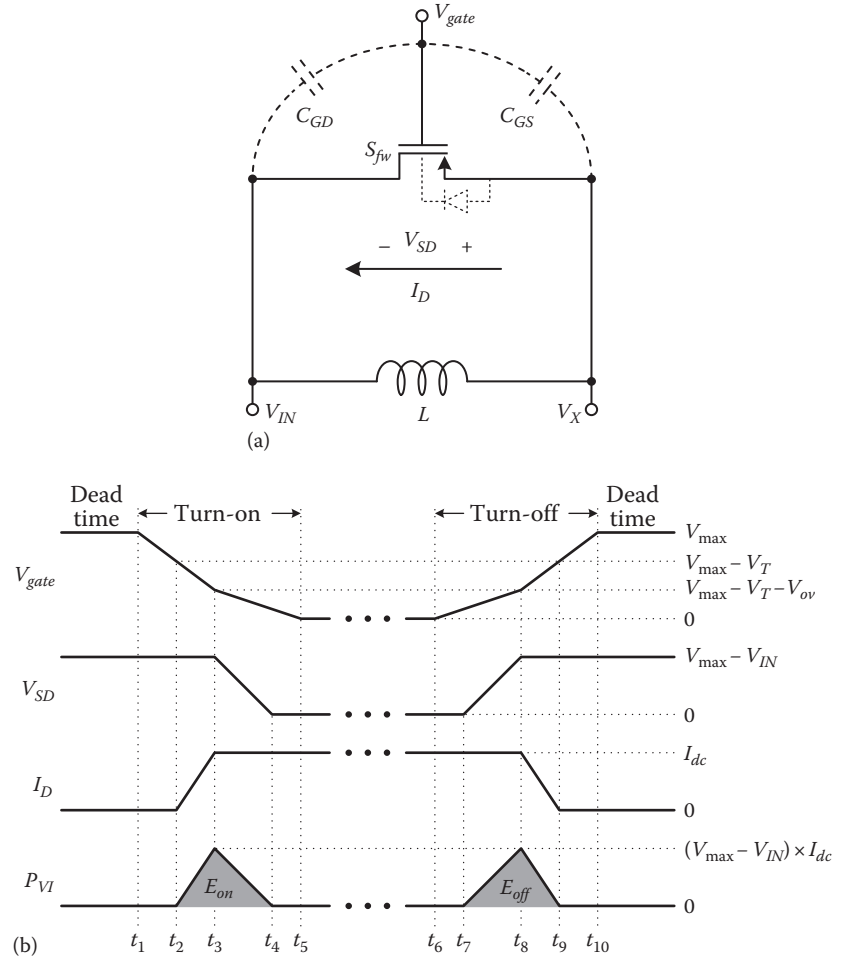

FIGURE 3.10 (a) Circuit model and (b) key waveforms for switching power loss. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

The process ends when V_{gate} becomes zero at t_5. The *V–I* overlap from t_2 to t_4 results in the corresponding energy loss E_{on}. This is calculated as

$$E_{on} = \frac{1}{2}(V_{\max} - V_{IN}) \cdot I_{dc} \cdot (t_{IR} + t_{VF}), \tag{3.9}$$

where t_{IR} and t_{VF} are the current rising time ($t_3 - t_2$) and voltage falling time ($t_4 - t_3$), respectively. Similarly, the turn-off transition reverses the sequence of the events and generates the turn-off *V–I* overlapping energy loss

$$E_{off} = \frac{1}{2}(V_{\max} - V_{IN}) \cdot I_{dc} \cdot (t_{VR} + t_{IF}), \tag{3.10}$$

where t_{VR} and t_{IF} are defined as the voltage rising time ($t_8 - t_7$) and current falling time ($t_9 - t_8$), respectively. For multiple-charge SIMO converters in PCCM, S_{fw} switches n times per switching cycle. The overall V–I overlap power loss is

$$P_{VI} = \frac{1}{2}(V_{\max} - V_{IN}) \cdot I_{dc} \cdot (t_{IR} + t_{VF} + t_{VR} + t_{IF}) \cdot n \cdot f_{sw}, \tag{3.11}$$

where f_{sw} is the switching frequency of the converter.

Another major switching power loss is the gate-drive power loss. This involves the charge/discharge processes on gate capacitors C_{GD} and C_{GS}. For C_{GD}, the drain terminal is constantly connected to V_{IN} and the gate voltage swings between $V_{\max}$ and zero, leading to a traversed voltage of $V_{\max}$. But for C_{GS}, the voltage of source terminal (V_X) is tied to V_{IN} during the conduction period and $V_{\max}$ during the dead times. Meanwhile, the gate voltage is equal to zero and $V_{\max}$, respectively. The traversed voltage of C_{GS} is then calculated as V_{IN}. The gate-drive loss of freewheel switch can be derived as

$$P_{DRV} = (C_{GD} \cdot V_{\max}^2 + C_{GS} \cdot V_{IN}^2) \cdot n \cdot f_{sw}. \tag{3.12}$$

The total switching power loss of S_{fw}, thus, can be denoted as

$$P_{SW} = \left[\frac{1}{2}(V_{\max} - V_{IN}) \cdot I_{dc} \cdot (t_{IR} + t_{VF} + t_{VR} + t_{IF}) + (C_{GD} \cdot V_{\max}^2 + C_{GS} \cdot V_{IN}^2)\right] \cdot n \cdot f_{sw}. \tag{3.13}$$

In conclusion, to achieve high efficiency in a SIMO converter operating in PCCM, the conduction and switching losses of the freewheel switch should be jointly minimized. These power losses are highly related to switching frequency of S_{fw}, freewheel switching current I_{dc} and freewheel switching period.

3.6.2 Adaptive PCCM Operation Schemes

To identify the optimal operation point, Figure 3.11 illustrates the inductor current I_L in different operation conditions. The proposed adaptive PCCM operation scheme aims to provide a universal method to maintain this optimization in different load conditions. It should be noted that in any case each freewheel switching period should not be too short in order to prevent the converter from entering CCM. Neither should it be too long to cause large conduction loss. This is easy to achieve in balanced load conditions such as in Figure 3.11a. However, in unbalanced load conditions as in Figure 3.11b, due to the fixed phase durations, the freewheel switching period for the light-load output ($D_{fw2}T$) becomes much longer. The conduction loss of S_{fw}, thus, increases significantly. A straightforward way to reduce it is to lower the freewheel switching I_{dc} level. However, since the phase durations are fixed, this may cause the other subconverter to enter CCM (Figure 3.11c), resulting in cross-regulation. Therefore, to maintain the optimal freewheel switching duration for each subconverter, both the phase durations and I_{dc} level should be adaptively controlled (Figure 3.11d).

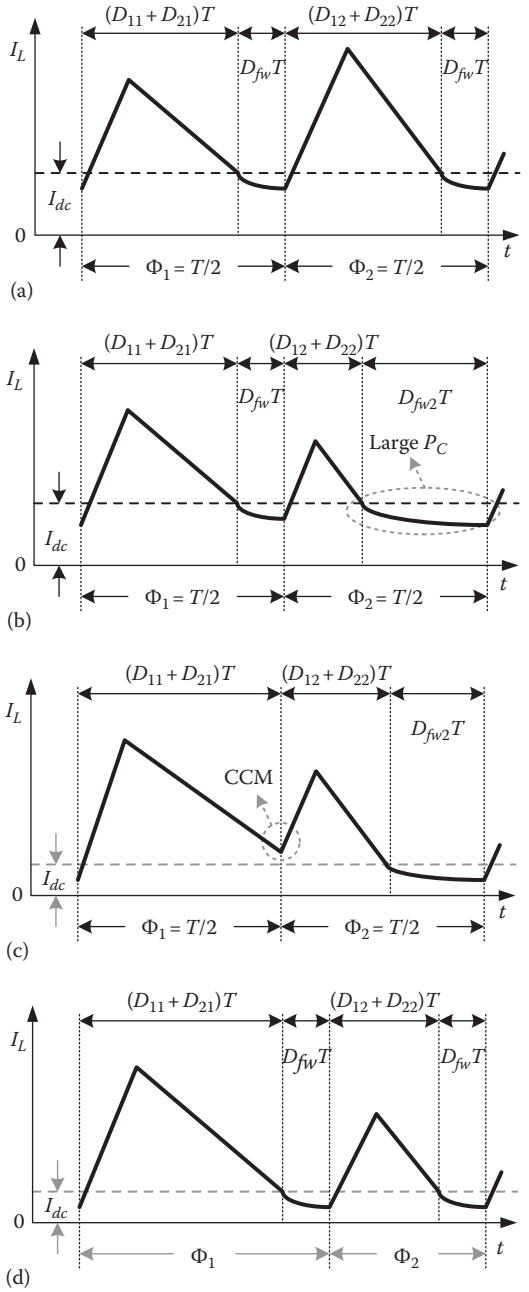

FIGURE 3.11 Inductor current waveform in pseudo-continuous conduction mode with (a) balanced loads, (b) unbalanced loads, (c) lowered I_{dc}, and (d) adaptively controlled phase durations and I_{dc}. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

3.6.2.1 Adaptive PCCM with Distributed Freewheel Switching

The adaptive PCCM operation scheme with distributed freewheel switching is illustrated in Figure 3.12. Initially, the two phases of a SIDO converter are set equally as $T/2$, with a preset freewheel switching current at I_{dc}. The duration of $\Sigma D_{ki}T$ is defined as

$$\sum D_{ki}T = \sum_{k=1}^{2} D_{ki}T = (D_{1i} + D_{2i})T. \tag{3.14}$$

If the load current I_{LOAD1} of subconverter 1 suddenly increases (case (ii) in Figure 3.12), $\Sigma D_{k1}T$ is extended by ΔDT to accommodate this load power increase, resulting in a decreased freewheel switching duration in Φ_1. The two freewheel switching periods

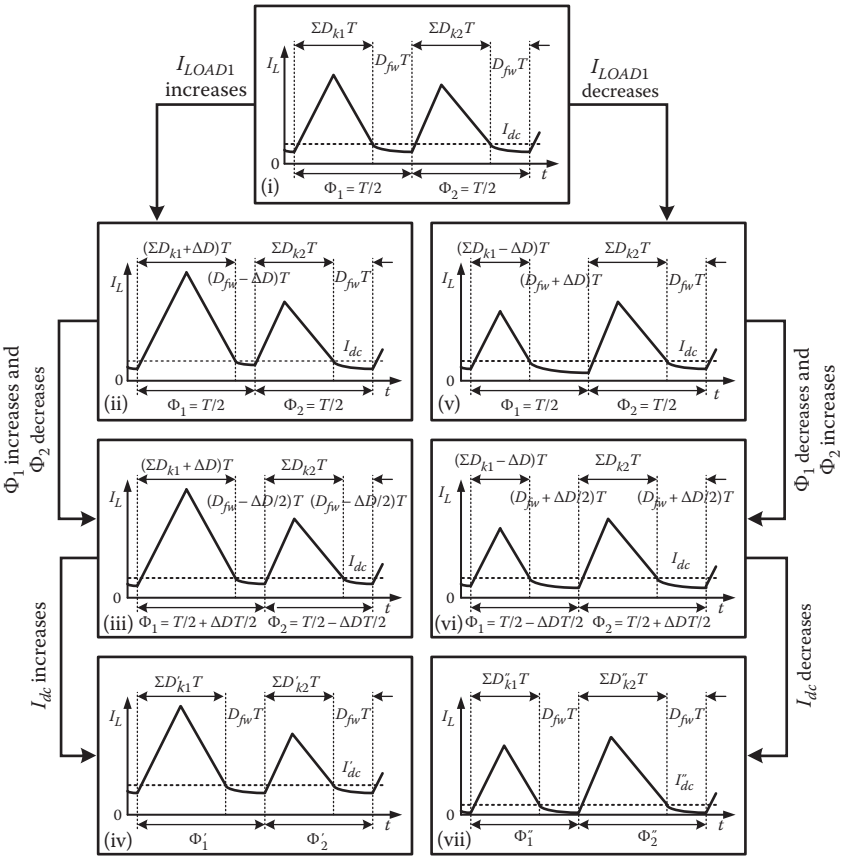

FIGURE 3.12 Adaptive pseudo-continuous conduction mode operation scheme with distributed freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

are then equalized by adjusting the phase durations Φ_1 and Φ_2 in case (iii). Since this average freewheel switching duration is smaller than the optimal value, the I_{dc} level is gradually increased to prolong the freewheel switching periods. Thus, the phase adjustment and I_{dc} modulation take place iteratively to maintain the optimal freewheel switching durations. Similar actions apply when I_{LOAD1} suddenly decreases. To quantize the relation between phase duration, I_{dc}, and the instant loads, the inductor current for a SIMO converter in PCCM with distributed freewheel switching is reexamined in Figure 3.13. Here, the ratio of D_{1i} to D_{2i} is defined by

$$\frac{D_{1i}}{D_{2i}} = \frac{m_{2i}}{m_{1i}}, \tag{3.15}$$

where m_{1i} and m_{2i} are the slopes of I_L and can be defined as

$$\begin{cases} m_{1i} = \dfrac{V_{IN}}{L} \\ m_{2i} = \dfrac{V_{Oi} - V_{IN}}{L} \end{cases}. \tag{3.16}$$

On the other hand, the total charge delivered to the ith output per switching cycle is calculated as

$$Q_i = I_{dc} \cdot D_{2i}T + \frac{m_{2i}}{2} \cdot (D_{2i}T)^2. \tag{3.17}$$

In steady state, it equals to the total charge demanded by the load I_{LOADi}, which gives

$$Q_i = I_{LOADi} \cdot T. \tag{3.18}$$

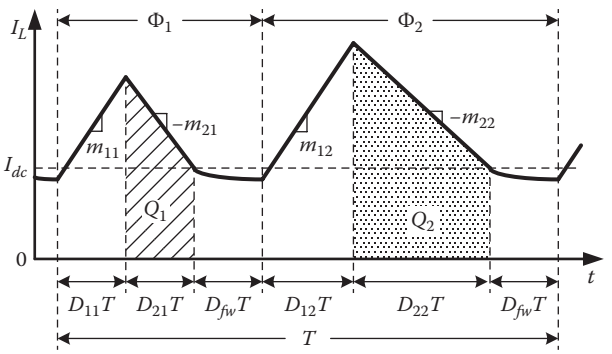

FIGURE 3.13 I_L with distributed freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

Substituting Equation 3.18 into Equation 3.17 gives

$$D_{2i}T = \frac{\sqrt{I_{dc}^2 + 2m_{2i}T \cdot I_{LOADi}} - I_{dc}}{m_{2i}}. \tag{3.19}$$

Based on Equations 3.15 and 3.19, the adaptive adjustment on each phase duration follows

$$\Phi_i = \frac{m_{1i} + m_{2i}}{m_{1i} \cdot m_{2i}} \left(\sqrt{I_{dc}^2 + 2m_{2i}T \cdot I_{LOADi}} - I_{dc} \right) + D_{fw}T. \tag{3.20}$$

3.6.2.2 Adaptive PCCM with Unified Freewheel Switching

Alternatively, unified freewheel switching can be implemented, where the freewheel switching only occurs once per switching cycle. According to Equation 3.13, the switching power loss of S_{fw} can be reduced (Zhang and Ma 2011). This saving can be significant when the number of the subconverters in a SIMO converter is large.

Here, a SIDO converter is employed as an example. If I_{LOAD1} suddenly increases from the steady state in case (i) in Figure 3.14, the corresponding phase duration of Φ_1 is extended by $\Delta D_1 T$ to allow more inductor current to be delivered to V_{O1}, thereby stabilizing V_{O1}. Because of using the same start and end levels of the I_{dc}, Φ_2 is time-shifted until I_L in Φ_1 returns to I_{dc}. The duration of Φ_2 remains the same (as in case (ii)). Hence, the total current delivered to V_{O2} in each switching cycle remains unchanged through the adjustment on the duration of the freewheel switching. At the end, the variation $\Delta D_1 T$ is completely absorbed through the freewheel

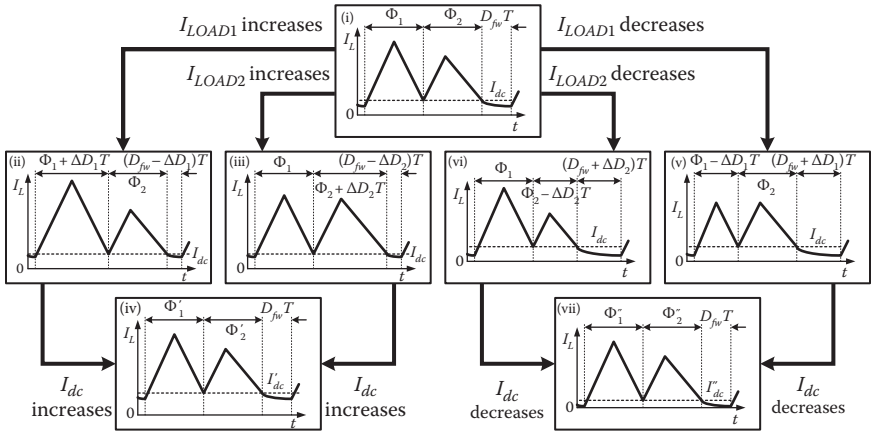

FIGURE 3.14 Adaptive pseudo-continuous conduction mode operation scheme with unified freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

switching with a shorter freewheel switching duration $(D_{fw} - \Delta D_1)T$ in case (ii). Similar adaptive operation process can be applied when I_{LOAD2} increases, as shown in case (iii). Conversely, if one load current is suddenly decreased, the corresponding phase duration will be reduced and the freewheel switching period will be prolonged (cases (v) and (vi) of Figure 3.14). It should be noted that, as the regulation period for each subconverter is not isolated from each other, risk of cross-regulation exists in this scheme.

In addition, the freewheel switching current level I_{dc} also needs to be adjusted to maintain the optimal freewheel switching duration. In the proposed operation scheme, if the monitored freewheel switching duration is shorter than the desired value (cases (ii) and (iii) in Figure 3.14), the freewheel switching current will be gradually increased from I_{dc} to a higher level I'_{dc}, thereby recovering the optimal value of $D_{fw}T$ (case (iv) in Figure 3.14). This adjustment prevents the freewheel switching duration from disappearing (CCM) when a sudden load change occurs. Similarly, the freewheel switching current gradually decreases to a lower I''_{dc} (case (vii) in Figure 3.14) when the freewheel switching duration is longer than the desired value (cases (v) and (vi) in Figure 3.14). It should be noted that the duration ratio between Φ'_1 (Φ''_1) and Φ'_2 (Φ''_2) in case (iv) (case (vii)) depends on the previous condition in case (ii) (case (v)) or case (iii) (case (vi)). Similarly, to quantize the relation between phase duration, I_{dc}, and instant loads, the control equation can be obtained from Figure 3.15 such that

$$\Phi_i = \frac{m_{1i} + m_{2i}}{m_{1i} \cdot m_{2i}} \left(\sqrt{I_{dc}^2 + 2m_{2i}T \cdot I_{LOADi}} - I_{dc} \right). \tag{3.21}$$

3.6.3 System Architecture and Circuit Design

The proposed adaptive PCCM operations schemes are suitable for both digital and analog implementations. As digital design is usually portable to technology scaling and backed up by well-designed electronic design automation (EDA) tools, it always

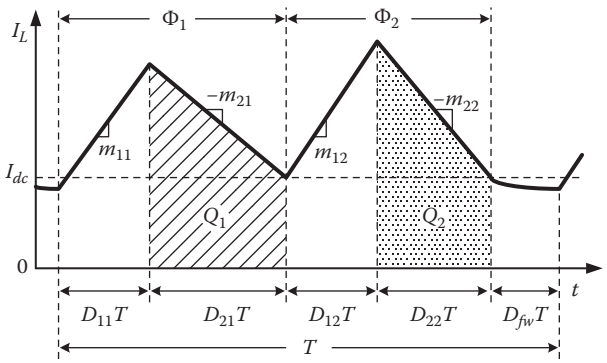

FIGURE 3.15 I_L with unified freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

carries a great commercialization potential. Hence, a digital implementation is introduced first using the distributed freewheel switching scheme as major control algorithm. On the other hand, in many cases, analog approach can be very efficient in the aspects of silicon and power consumption. An analog implementation using unified freewheel switching scheme is, thus, discussed as well. In general, the proposed schemes are flexible to either digital or analog processing and can be virtually implemented in any fabrication processes.

3.6.3.1 Implementation of Digital Adaptive PCCM

Figure 3.16 shows the system block diagram of a SIDO boost converter, with the control scheme proposed in Section 3.6.2.1. The operation can be described with reference to Figure 3.17. Consider a SIMO converter has n subconverters. Initially, the phase period for each subconverter and freewheel switching I_{dc} levels are set equal ($\Phi_1 = \Phi_2 = \cdots = \Phi_n$). As the load differs at each output, the freewheel switching duration in each phase differs accordingly.

Such a freewheel switching duration $D_{fwi}T$ ($1 \le i \le n$) is measured by a high-frequency digital counter, which also computes the average freewheel switching

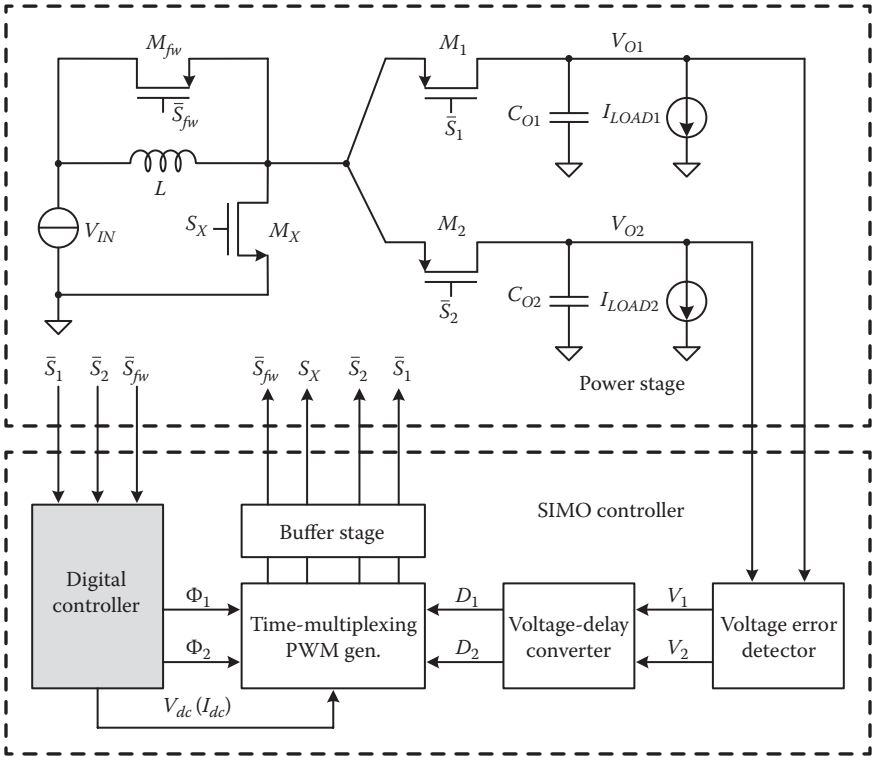

FIGURE 3.16 Block diagram of an adaptive pseudo-continuous conduction mode single-inductor dual-output boost converter with digital distributed freewheel switching. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

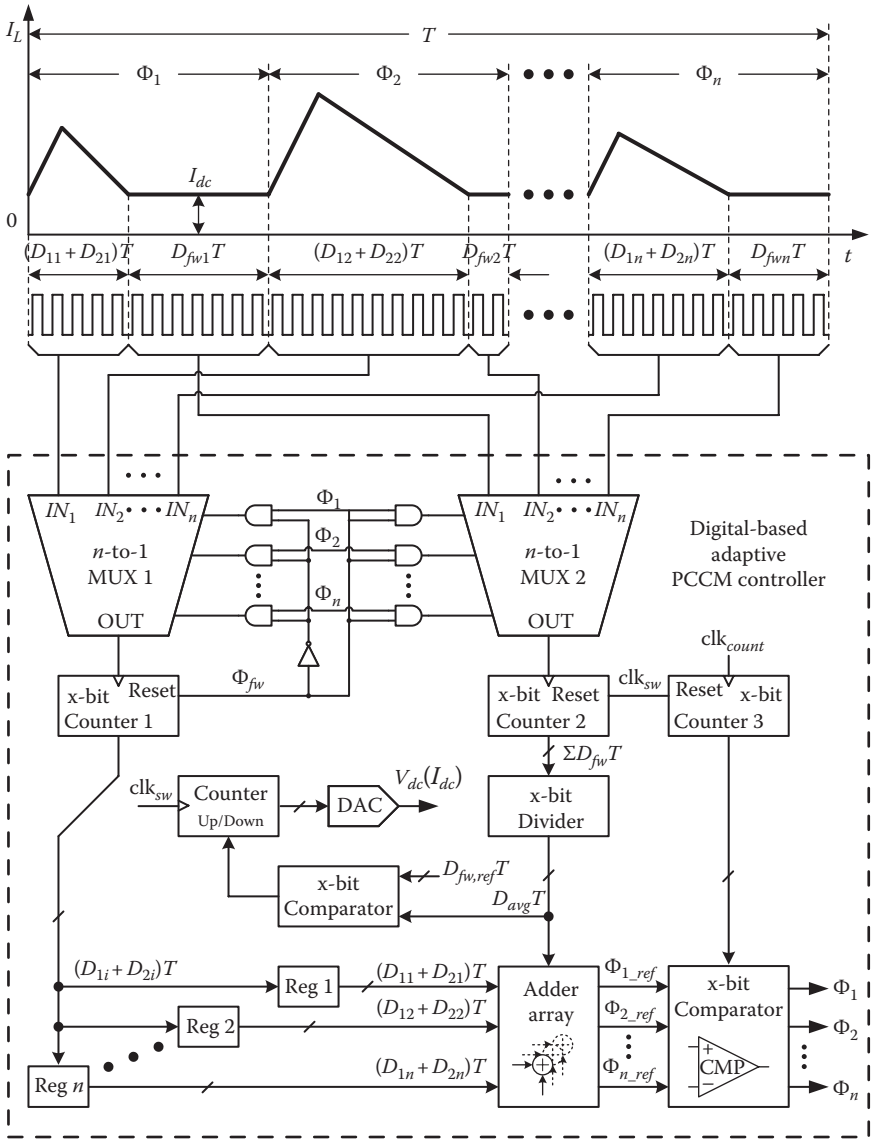

FIGURE 3.17 Implementation of the digital controller with timing diagram. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

duration $D_{avg}T$ ($=\sum D_{fwi}T/n$). Each charge and discharge period $(D_{1i} + D_{2i})T$ is also measured. By adding $D_{avg}T$ to $(D_{1i} + D_{2i})T$, the phase duration Φ_i for subconverter i in the next switching cycle is updated as

$$\Phi_i = (D_{1i} + D_{2i} + D_{avg})T. \tag{3.22}$$

In practice, the $D_{avg}T$ should not be too long in order to reduce conduction loss according to Equation 3.8. If it is longer than a predefined limit $D_{fw,\max}T$, the adjustment on freewheel switching I_{dc} will be activated. I_{dc} is then decreased by a step of $(I_{dc,\max} - I_{dc,\min})/2^x$ for each cycle, where x represents the number of bits in the digital-to-analog converter (DAC) of Figure 3.17. As I_{dc} decreases, $(D_{1i} + D_{2i})T$ extends to keep the delivered current to be the same as in the last switching cycle. As a result, the freewheel switching periods $D_{fwi}T$ in all subconverters decrease to reduce $D_{avg}T$ to be shorter than $D_{fw,\max}T$. Similarly, reverse adjustment steps will be taken if $D_{avg}T$ is smaller than $D_{fw,\min}T$, which is at high risk of cross-regulation. Once the instant $D_{avg}T$ falls between $D_{fw,\min}T$ and $D_{fw,\max}T$, I_{dc} adjustment is then completed. The iterative averaging on $D_{fwi}T$ leads the optimal operation eventually.

3.6.3.2 Implementation of Analog Adaptive PCCM

The adaptive PCCM operation scheme with unified freewheel switching is demonstrated through an analog implementation. In addition to the error amplifiers EA_i to determine the peak inductor current for each subconverter, the analog controller includes an online analog charge meter to adaptively adjust I_{dc} level, as shown in Figure 3.18. The inductor current is sensed by monitoring the currents flowing through M_X, M_1, and M_2, which are then converted to voltage signals and compared with V_{EAOi} and V_{dc}, thereby defining the duty ratios, phase durations, and freewheel switching durations. To explain the operating mechanism, a key voltage V_{dc} highlighted in Figure 3.18 is illustrated in Figure 3.19.

During the discharge period of $D_{2i}T$ in subconverter i ($i = 1$ or 2), C_{dc} in Figure 3.18 is charged by a constant current I_{ch}. When a freewheel switching action occurs, a constant sink current I_{dch}, which is equal to $m \times I_{ch}$, is activated to discharge C_{dc}. In steady state (solid line in Figure 3.19), it satisfies

$$I_{ch} \cdot (D_{21}T + D_{22}T) = I_{dch} \cdot D_{fw}T. \tag{3.23}$$

V_{dc} keeps constant and an optimal freewheel switching duration can be achieved by setting an appropriate m value. If a load increase occurred in the last phase (Figure 3.19a), the corresponding charge and discharge periods of inductor current ($D'_{12}T$ and $D'_{22}T$) need to be extended in order to deliver more power. The freewheel switching duration ($D'_{fw}T$) is reduced accordingly, resulting in

$$I_{ch} \cdot (D'_{21}T + D'_{22}T) > I_{dch} \cdot D'_{fw}T. \tag{3.24}$$

Consequently, V_{dc} is increased to V'_{dc} and a higher I_{dc} level is thus achieved. Similarly, when a load decrease occurs, V_{dc} decreases due to

$$I_{ch} \cdot (D''_{21}T + D''_{22}T) < I_{dch} \cdot D'''_{fw}T, \tag{3.25}$$

leading to a lower I_{dc} level. On the other hand, when a load change occurs in the foregoing phase (Figure 3.19b), $D_{11}T$ and $D_{21}T$ show similar variations. Since the phase

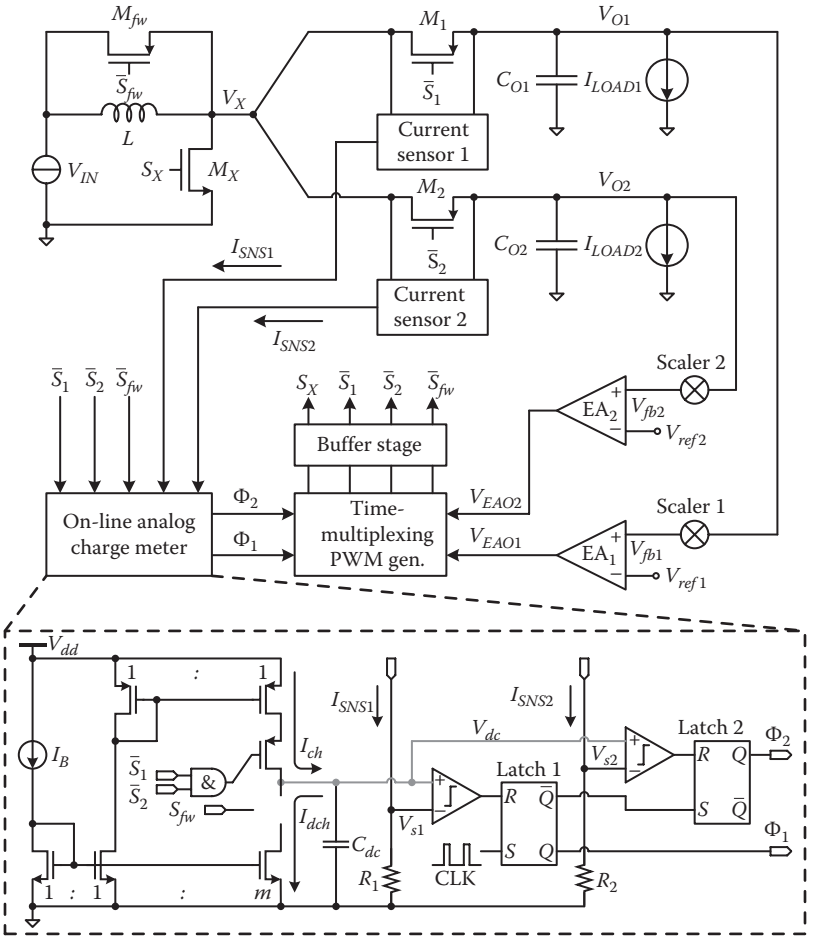

FIGURE 3.18 Circuit detail of single-inductor dual-output converter with proposed analog controller. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

duration of subconverter 2 keeps constant (Φ_2, Φ_2', and Φ_2'' are all equal), the variations are added to the freewheel switching period at the end of the switching cycle, thereby adjusting V_{dc} accordingly. With this method, I_{dc} can be adaptively adjusted based on instantaneous load condition, thus improving the conduction loss. Moreover, the frequency of freewheel switching actions is significantly reduced, leading to the reduction of switching power loss.

After the V_{dc} level is stabilized, the phase duration Φ_i of each subconverter is also automatically adjusted by the online charge meter. As shown in Figure 3.18, latch 1 is set by the clock signal *CLK* at the switching frequency of the SIMO converter. The discharge inductor current is sensed and converted to voltage signal V_{s1}. Once V_{s1} becomes lower than V_{dc}, Φ_1 expires and Φ_2 is initiated by latch 2. Similarly, Φ_2 expires when I_L ramps down to I_{dc} level.

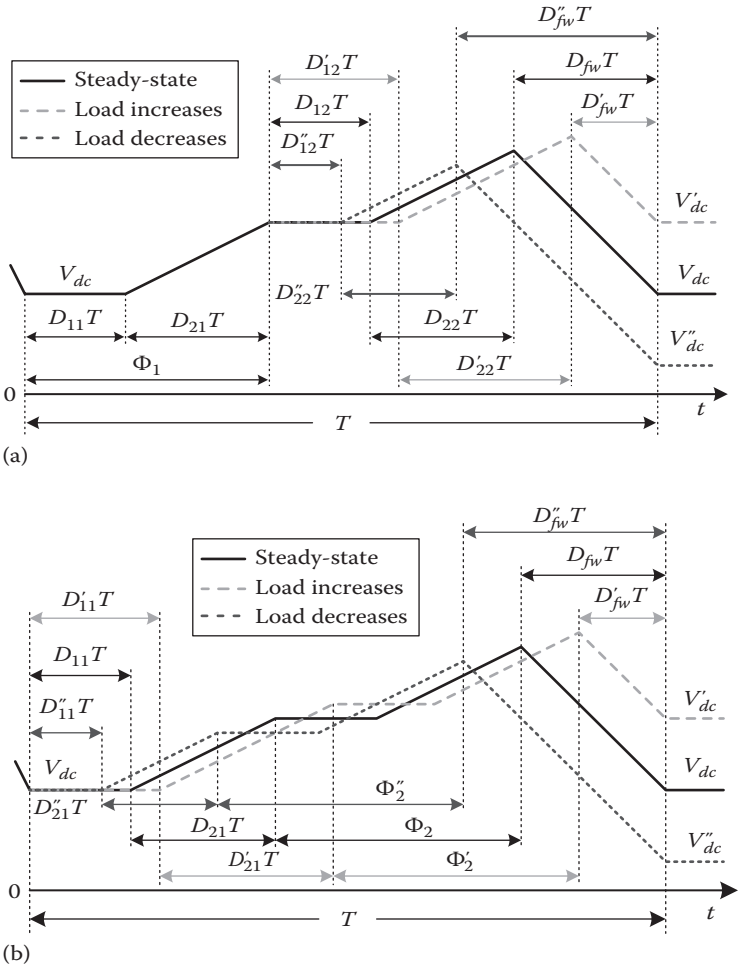

FIGURE 3.19 V_{dc} adjustment with load variation occurring in (a) the last phase and (b) the foregoing phase. (From Zhang, Y. and Ma, D., *J. Analog Integr. Circuits Signal Process.*, 72(2), 419, August 2012b.)

3.7 CONCLUSIONS

In this section, two adaptive PCCM operation schemes with the respective distributed and unified freewheel switching schemes were discussed. Compared with conventional PCCM operations, the phase durations and I_{dc} level can be adaptively modulated, thereby maintaining optimal freewheel switching in various load conditions. As a result, power loss due to freewheel switching can be significantly reduced while retaining low cross-regulation effect. In addition, the two proposed operation schemes were implemented by both digital and analog methods. The advantages for each implementation method are also discussed respectively.

For the digital implementation, as most of the control circuits consist of the robust digital circuits, the system robustness across the process, voltage, and temperature (PVT) variations can be significantly improved. Moreover, with the development of modern VLSI techniques, digital circuits usually consume less silicon area compared with analog circuit counterparts.

On the other hand, by using the analog implementation method, the I_{dc} level and phase durations for adaptive PCCM operation can be accurately fine-tuned. The adjustment resolution is thus well improved, resulting in more accurate control scheme. Based on the specific application background, the digital and analog circuit implementation, as well as the distributed/unified freewheel switching, can also be combined in different ways to define the most appropriate adaptive PCCM operation scheme for SIMO converters.

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